CU SERVICE MANUAL

(Preliminary Version)

for

P850 - P855 - P860

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PREFACE

This manual contains the logic and special circuits information needed to service the Device Control Unit (DCU) cards produced by Philips for the P800 series of Mini-Computers. The manual is divided into sections and each section except the first deals with a specific DCU.

The first section deals with the I/O bus and its timing and with the operation of DCU's in general. This section is applicable to all the DCU's included in the following sections.

All the remaining sections deal with specific DCU's and their operation. The last page of each section is a fold-out logic diagram that also includes information on the special circuits. Each diagram has grid reference points marked on it to enable easy location of the various logic elements described in the text. These reference points should not be confused with similar reference points etched on the DCU cards, that are used to identify the logic elements.

The information contained in this book is based on the documentation available at the time of printing 1st December 1971. However, should any user wish to make any suggestion for improving this manual, he is invited to send his comments to:

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SECTION I

INTRODUCTION

All the Control Unit (CU) cards described in this manual operate in a similar way and the information in this section i s applicable to all of them. They are the interface between the CPU and the peripheral device and translate I/O instructions into mechanical actions of the device and provide the sequencing and control signals to effect data transfers.

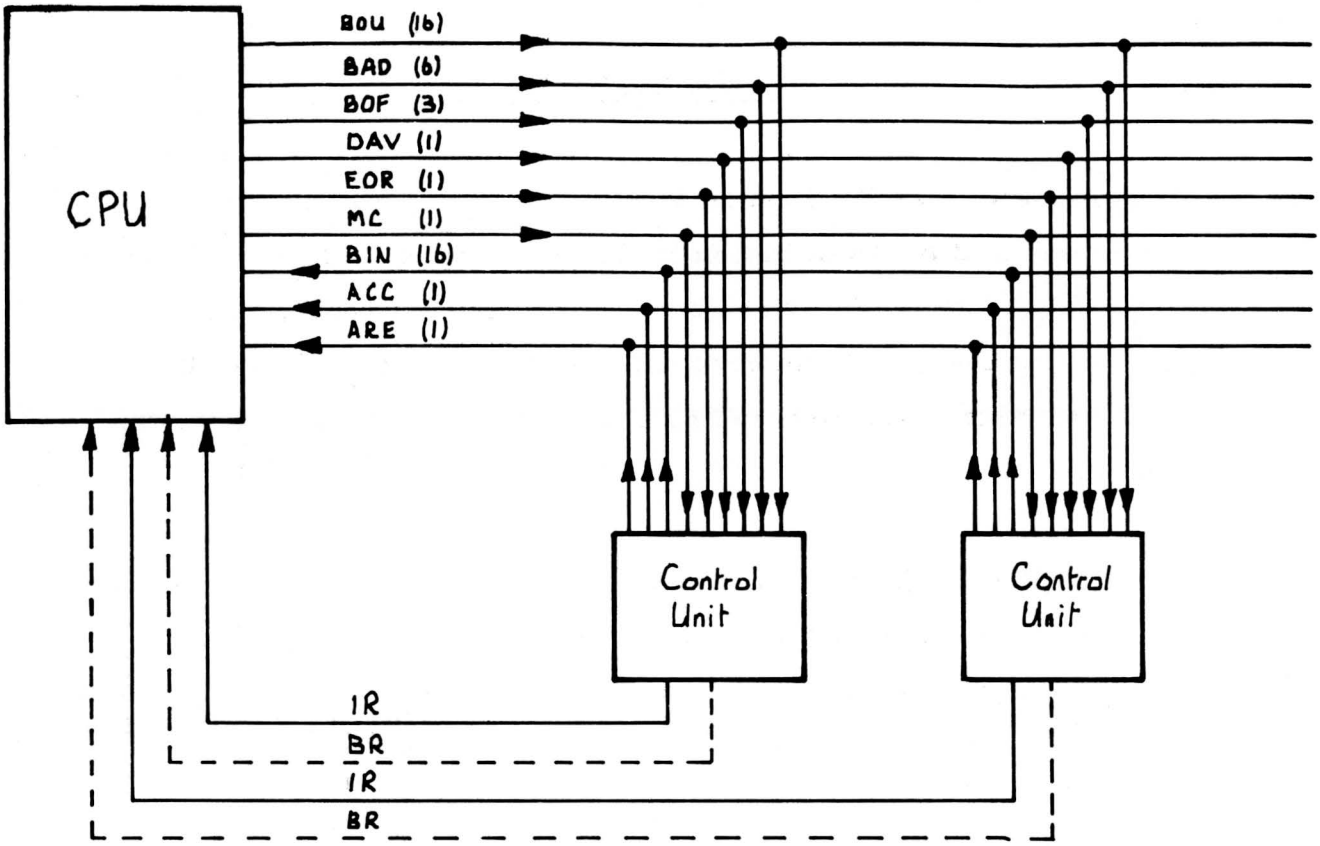
1.2 I/O BUS Communication between the CPU and the CU is via the I/O bus; its lines being hard wired to the sockets reserved for CU cards. Figure 1.1. shows the connection of CU cards to the bus and up to 32 CU cards can be connected to the I/O bus.

1.3 COMMANDS The commands sent to a CU will be:

(i) CIO - To start or stop a transfer,
(ii) INR - To effect a transfer from a device to the CPU,
(iii) OTR -To effect a transfer from the CPU to the device,
(iv) TST - To test the status of the device before starting or during any transfer,
(v) SST - To test the status of the device after the transfer has been completed.

These commands originate in the I/O instructions and will include the address of the device.

1.4 ADDRESSING. The CU address is sent via the BAD lines of the I/O bus. Each CU card will have a BAD input gate that will only recognize its own address. The code for this address will have been wired up on the pinboard of each CU card. Some CU cards can control more than one device, and these cards have the address of each device wired up on their pinboard.



Key:

CPU Output
- BOU ... Output data bus (16 lines)
- BAD ... Device Address bus (6 lines)
- BOF ... Operation Function bus (3 Lines)
- DAV ... Device Address Valid bus
- EOR ... End of Range bus *

CU Output
- BIN ... Input data bus (16 lines)
- ACC ... Accept Command line
- ARE ... Address Recognised line
- IR ... Interrupt Request line
- BR ... Break Request line *

* Only used with Multiplex transfers

Figure 1.1. CU to I/O Bus Connection

1.5 FUNCTION CODE This code contains the actual command to the CU and is sent via the BOF lines of the I/O bus. The three bits of the code are translated into a command which is sent to the device via the sequence control part of the CU. The following table shows the decoded bits translated into commands:

Instruction	Bit 4	Bit 8	Bit 9	Command
CIO	0	1	1	Start
CIO	0	1	0	Stop
INR	1	0	0 or 1	Input Transfer
OTR	0	0	0 or 1	Output Transfer
TST	1	1	n/s	Test Status
SST	1	1	1	Sense Status

These commands will only be accepted if the control signals have validated the address and the CU sequence logic is in the right mode.

1.6 CONTROL SIGNALS There are three control signals lines from the CPU to the CU and two control signal lines from the CU to the CPU contained in the I/O bus. In addition there will be the Interrupt and/or the Break Request lines from the CU to the CPU.

DAV This signal is used to validate data on the BAD and BOF lines. If the address on the BAD lines is recognized, the CU will respond with the ARE signal and if the command on the BOF lines is accepted it will respond with the ACC signal.

MC This is the Master Clear signal that is activated either from the CPU control panel or the power supply each time the CPU is switched on.

EOR This is the End of Range signal which is sent at the end of a Multiplex transfer.

ARE This signal is sent to the CPU when the address on the BAD lines has been accepted by the CU.

ACC This signal is sent to the CPU when the command on the BOF lines has been accepted.

INTERRUPT and BREAK REQUEST These signal lines connect each discrete CU to the CPU interrupt system. The Interrupt line is used for programmed channel transfers, the Break Request line for multiplex transfers. Each is activated by the CU to indicate to the CPU that it is ready to exchange data or status information.

1.7 I/O BUS TIMING The timing of the I/O bus signals are shown in figure 1.2.

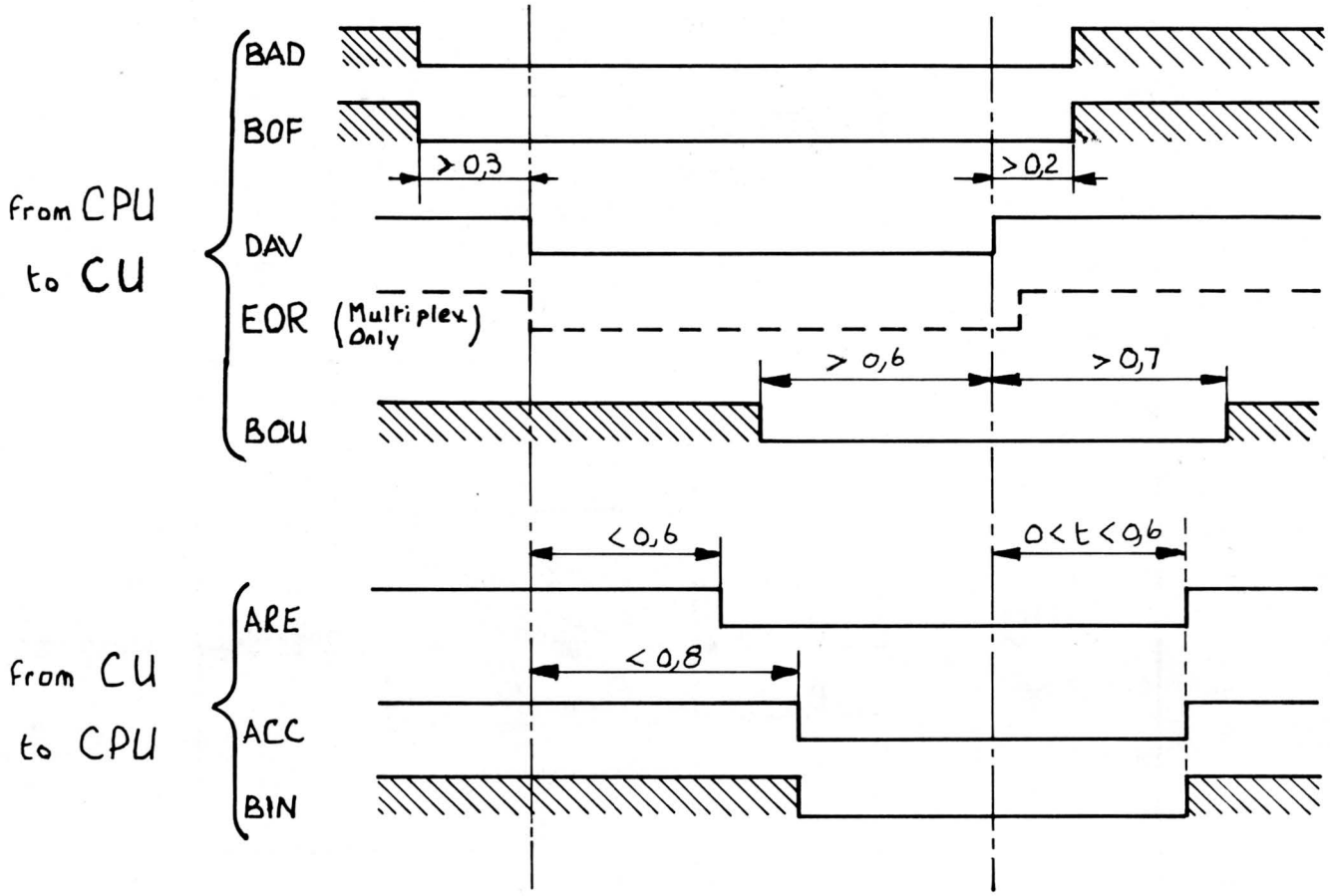
1.8 CU MODES Figure 1.3 shows a block diagram of a typical CU. Once the address has been accepted by the CU, a check is made to find out if the CU is in the right mode to accept the command on the BOF lines. The modes are:

INACTIVE The only commands accepted in this mode are CIO start and TST. In this mode a TST command will cause the CU to respond with zeros on all the BIN lines. A CIO Start command will cause the CU to switch from inactive to the Execute or Exchange modes depending upon whether the exchange is to be input or output.

EXECUTE This mode causes the device to perform a single mechanical action after which it switches the CU into either the Exchange or Wait Status modes. The only commands accepted in this mode are CIO Halt and TST. The CIO Halt will cause the CU to switch to the Wait Status mode. The TST will not affect the CU operation but will send a busy signal signal back to the CPU.

EXCHANGE This mode activates the Interrupt or Break Request line to indicate to the CPU that it is ready to receive or send data. After the exchange the CU will switch back to the execute mode. The only commands accepted in this mode are INR, OTR or TST. The INR will transfer data to the CPU via the BIN lines, the OTR will accept data from the BOU lines and the TST will send the CU status back to the CPU.

WAIT The CU goes into this mode after receiving a CIO Halt command whilst in the Execute mode. When the SST command has been accepted and serviced, it will switch to the Inactive mode. The only commands accepted in this mode are TST and SST. In both cases the CU sends the device status back to the CPU via the BIN lines;.

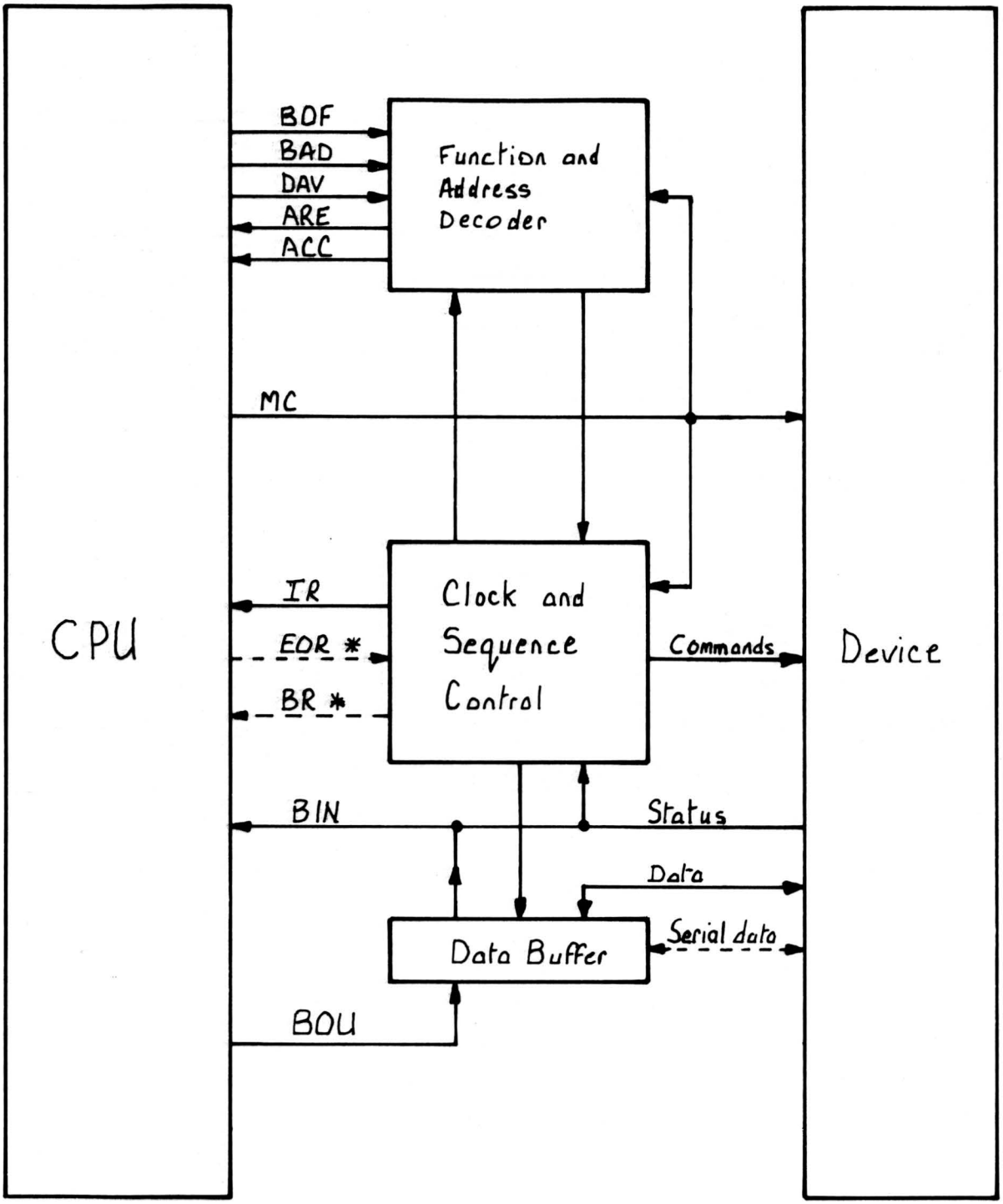


: Not defined

Times are given in microseconds

Low levels are active or data 1 except BOU where high level is data 1

Figure 1.2 I/O Bus Timing



* : Only used by multiplex

Figure 1.3 Block Diagram of Typical CU

1.9 MODES SEQUENCES The mode sequence depends on whether the transfer is input or output. Both sequences are shown in the flowchart in Figure 1.4.

1.10 CU AND DEVICE STATUS The status of the CU is tested by the TST command and the device status by the SST command.

TST This command is accepted by the CU in any mode. If the CU is in the Inactive mode (not busy) it will respond by sending all zeros to the CPU via the BIN lines. In any other mode (busy) it will respond by sending a 1 bit on BIN line 15 other lines are not significant.

SST This command is only accepted in the Wait mode and responds by sending the status of the device to the CPU via the BIN lines. The most common status bits are:

bit 15: Manual intervention required by the operator
bit 14: Throughput Error
bit 13: Data fault
bit 12: Incorrect length

Other bits may be used by the more sophisticated control units, but these will be given in the section dealing with these units.

1.11 I/O BUS CONNECTIONS

Connections to the pins of the I/O bus sockets have been standardised so that any DCU card can be plugged into any socket without modification. The list of connections and signal names is given below:

Socket		Socket	
1A01	+5V	2A01	BOF02/
1A02	reserved	2A02	EOR
1A03	BIN00/	2A03	BOF01/
1A04	BIN01/	2A04	BOF00/
1A05	BIN02/	2A05	BOU14
1A06	BIN03/	2A06	BOU13
1A07	BIN04/	2A07	BOU12
1A08	BIN05/	2A08	BOU09
1A09	BIN06/	2A09	BOU10

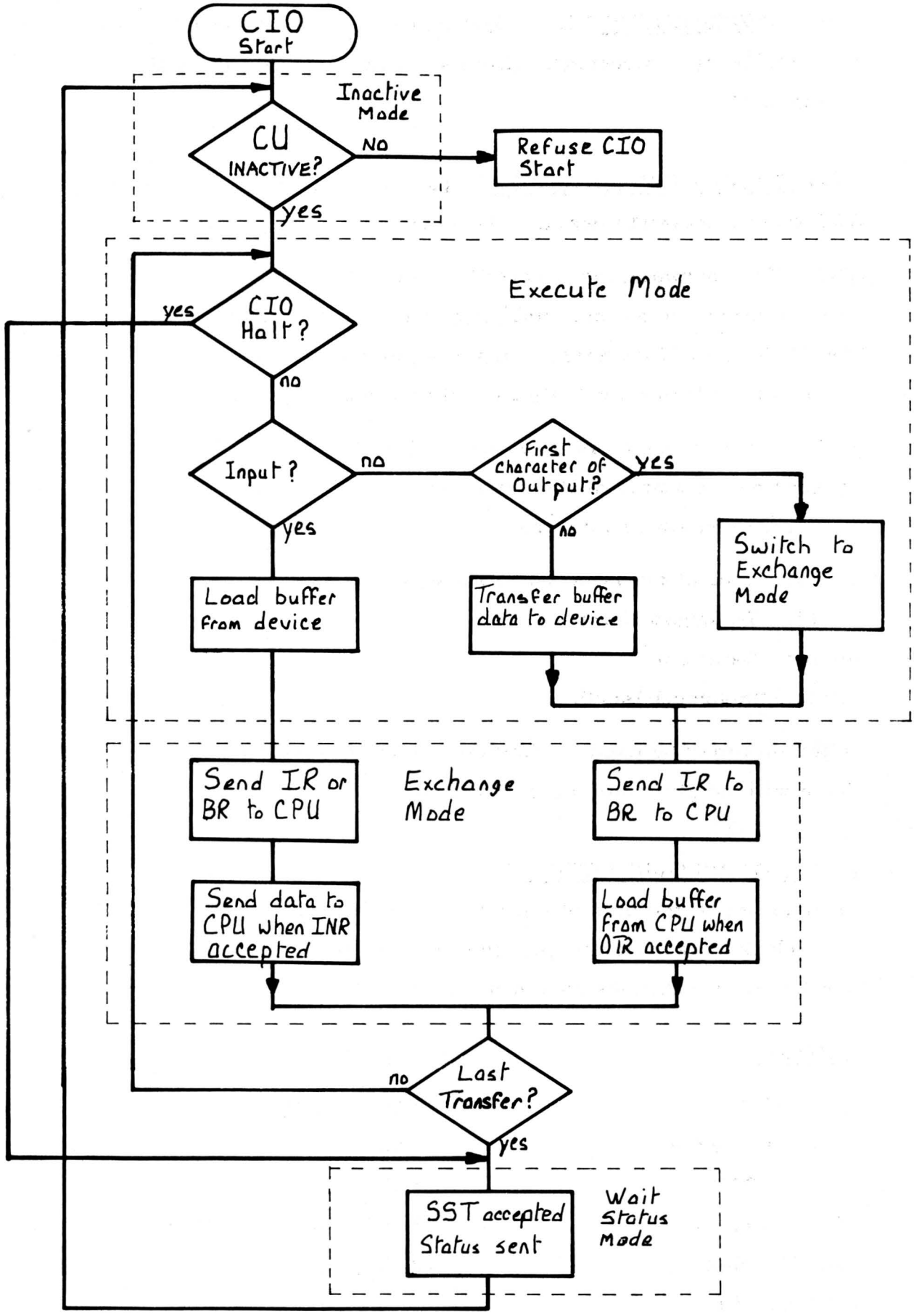


Figure 1.4 Mode Sequences

1A10	BIN07/	2A10	BOU11
1A11	ground	2A11	BOU15
1A12	reserved	2A12	MC/
1A13	ACC/	2A13	BAD03/
1A14	ARE/	2A14	DAV/
1A15	BRIR/	2A15	BAD04/
1A16	BR1/	2A16	BAD05/
1A17	BR2/	2A17	BOU08
1A18	BR3/	2A18	BOU07
1A19	BR4/	2A19	BOU06
1A20	reserved	2A20	BOU05
1A21	BIN08/	2A21	BOU04
1A22	BIN14/	2A22	BAD00/
1A23	+ 6 v	2A23	BOU03
1A24	- 6 v	2A24	BAD01/
1A25	- 12 v	2A25	BAD02/
1A26	BIN13/	2A26	BOU02
1A27	BIN15/	2A27	BOU01
1A28	BIN09/	2A28	BOU00
1A29	BIN10/	2A29	+ 24 v
1A30	BIN11/	2A30	- 5 v
1A31	BIN12/	2A31	+ 5 v
1B31	ground	2B31	ground

SECTION II

ASR CONTROL UNIT

BRIEF DESCRIPTION

The Control Unit (CU) logic and special circuits are contained on one card and will control one ASR. Its main function is to interface the parallel operation of the CPU I/O bus and the serial operation of the ASR. A clock circuit on the card provides the timing pulses necessary to effect transfers of data and to control the sequence of operation.

Standard I/O instructions are used to initiate data transfers and to send control signals to the ASR via the CU. The control signals are the start/stop signals to the Tape Reader and Tape Punch attached to the ASR. These signals are not generated by the CU but are programmed and transferred like any other data.

Figure 2.1 shows a block diagram of the main logic and special circuits of the ASR CU; the logic drawing for the CU card will be found in the pocket at the back of this book, a smaller logic drawing will be found at the end of this section. The smaller drawing has grid reference marks which are used in the text to enable the logic elements to be found quickly. The following paragraphs of this section describe the operation of the control unit in more detail, with the aid of these two diagrams.

2.1 ADDRESSING

The address of the CU card can be wired to recognize any address using the AD0 to AD5 (ref: A and B/1, a-3) switch connectors. When the CPU puts any CU address on the BAD lines, it validates it by sending the DAV (ref: A/1) signal. If the address corresponds to the code set up on the switch connectors, the CU responds by sending the ARE (ref: D/1-2) back to the CPU; this signal is also used to enable logic on the CU card.

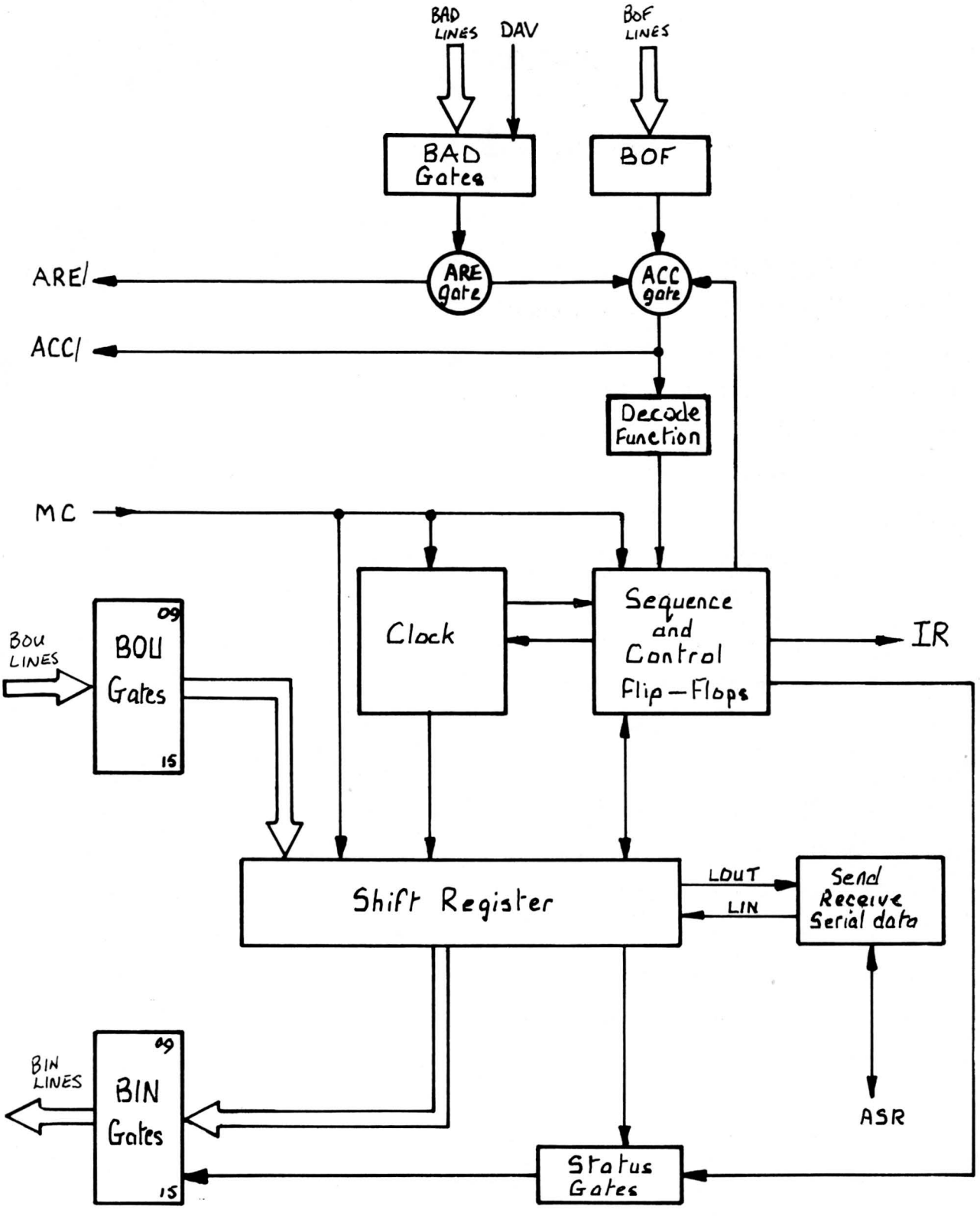


Figure 2.1 Block Diagram of ASR CU

2.2 BOF

Once the address has been recognized, the code on the BOF (ref: A and B/4-5) lines and the present state of the CU are checked to find out if the command can be accepted. If accepted the CU will send the ACC (ref: D/1) signal back to the CPU. At the same time the output from the function decode logic will enable the appropriate logic circuits in the CU to start execution of the command.

2.3 FUNCTION REGISTER

This register is made up of four flip-flops that store the type of function sent on the BOF lines. These flip-flops are:

FCA This flip-flop (ref: E and F/4) remembers that a CIO Start command has been accepted and performed. It enables the sequencer flip-flops to switch to either the Execute (EXT) state if the CIO was an input command, or to the Exchange (ECH) state if the CIO was an output command.

Set During the acceptance of the CIO start command.

Reset During acceptance of a CIO stop command.

(ii) At the beginning of any serialization.

(iii) During the exchange of data with the CPU.

FAOV This flip-flop (ref: F/4-5) remembers that either an INR or OTR command has been accepted and is used to enable the sequencer logic.

Set During any data exchange with the CPU.

(ii) During acceptance of an SST command.

Reset During execution of a Stop command.

(ii) During the Start of any I/O command execution

(iii) At the beginning of any serialization.

FHALT This flip-flop (ref: E/3) remembers that a stop command has been performed and enables the sequencer to switch to the Wait Status (WST) state if FSER is reset. It also inhibits any exchange request; remembers a detected throughput error and in conjunction with FAOV enables the sequencer to switch to the inactive (INCT) state after execution of an SST command.

Set During acceptance of a stop command.

(ii) During the serialization sequence (input) if a throughput error has been detected.

(iii) During the exchange state if the ASR is used on the multiplex chan channel.

Reset During the acceptance of an SST command.

FOUT This flip-flop (ref: B and C/8) controls the operating mode of the serializer circuit. When set it allows transfers from the CPU to the ASR, and when reset it allows transfers from the ASR to the CPU.

Set During the acceptance of a CIO Start command in output mode.

Reset During the acceptance of a CIO Start command in input mode.

2.4. CONTROL FLIP-FLOPS

These three flip-flops control the transfer of data between the CPU and the ASR. They are:

FSER This flip-flop (ref: E and F/6) enables serialization by starting the CU clock counting.

Set During input mode by the Start pulse from the ASR and during output mode by FFF/

Reset At the end of serialization by the trailing edge of the eleventh BP pulse

PE This flip-flop (ref: F and G/6) enables the shift register to either parallel load or one bit shift.

Set It is set by FSER

Reset By the trailing edge of the first AP pulse.

FTHR This flip-flop (ref: E/7) can detect a throughput error when the CU is in input mode.

Set When a new character tries to load the shift register whilst the CU is in the ECH state.

Reset During the acceptance of an I/O command.

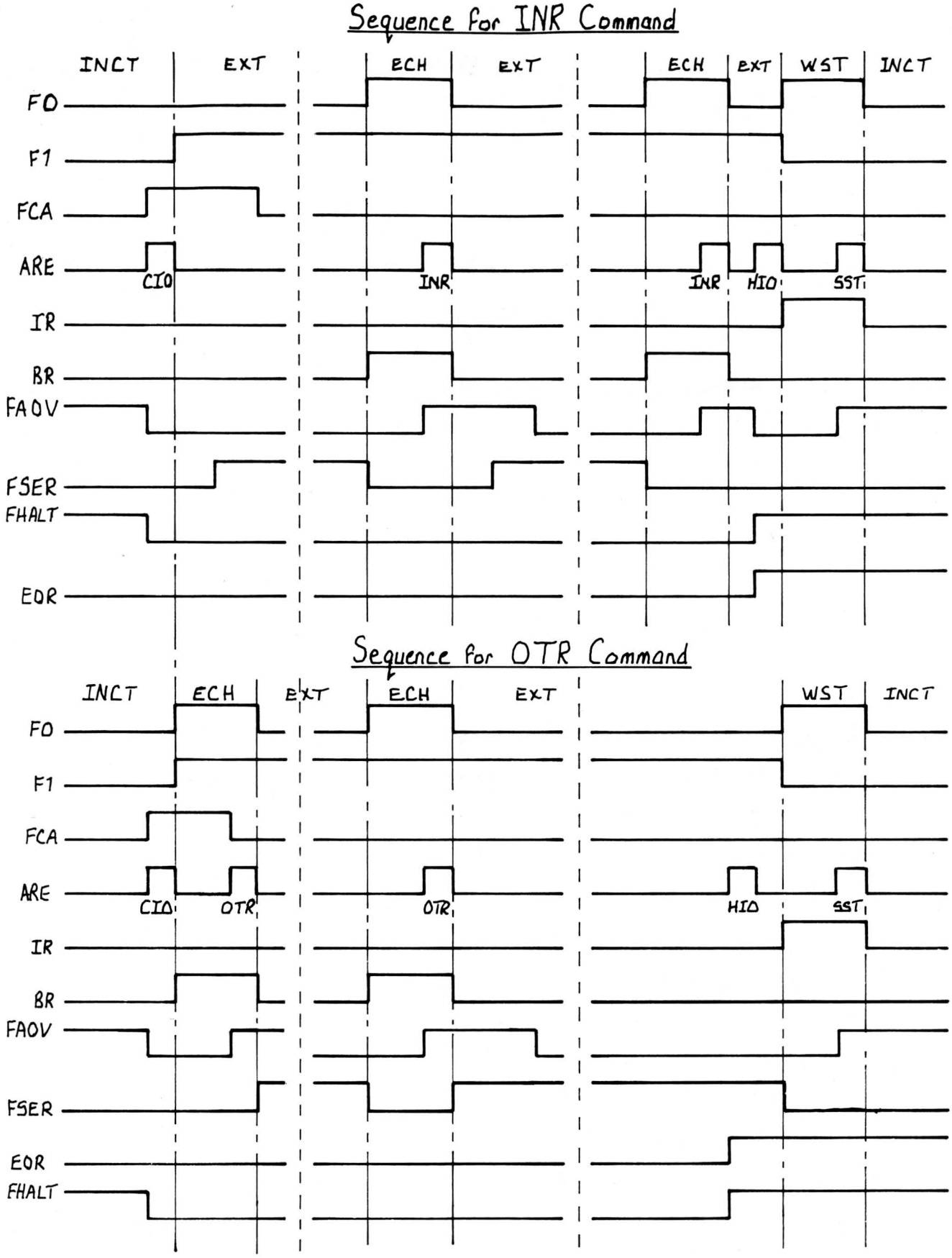
2.5 INTERFACE SEQUENCER

The sequencer uses two flip-flops F0 (ref: E and F/1-2) and F1 (ref: F/3) to switch the appropriate sequence states of the CU during data transfers. A combination of outputs from these flip-flops drives logic gates that provide the signal levels which indicate the state of the CU. These are:

(i) Inactive State (INCT) - F0/.F1/
(ii) Execute State (EXT) - F0/.F1
(iii) Exchange State (ECH) - F0.F1
(iv) Wait Status State (WST) - F0.F1/

2.6 SEQUENCER AND CONTROL TIMING

The timing for the sequencer and control flip-flops is dependant upon two other sources of timing signals; the I/O bus signals which are controlled by the CPU and the CU clock which controls transfers between the CU and the ASR. It is therefore not possible to draw a timing diagram that will relate the signals to the actual time taken for a transfer. However, figure 2.2. does show the relationship between the signals, in both input and output modes, during a data transfer.



Notes: 1. The section between the continuous dotted lines will be repeated as necessary until the end of data transfer.

2. EOR will only be used when the ASR is used on the Multiplex channel.
3. The IR and BR signals are "ored" together when the ASR is used on the I/O bus.

Figure 2.2 Sequence and Control Timing

2.7 CU CLOCK CIRCUIT AND TIMING

The clock provides timing pulses to synchronize the operation of the shift register and control logic of the CU to the speed of ASR distributor. The basic clock comprises the two monostable modules A3 and B4 (ref: B/6) which are interconnected to form a stable oscilator. Module A4 (ref: B/7) is used to give the correct pulse width to the two outputs. These outputs are used in conjunction with gates B4 (ref: B and C/7) to produce the biphase clock pulses AP and BP.

STARTING THE CLOCK The clock is started when signal FSER is rising after the flip-flop has been set.

STOPPING THE CLOCK The trailing edge of the eleventh BP pulse is used to reset FSER. The effect of FSER going low is taken through a delay network of gates C3 and B4 (ref: C/5-6) and used to stop the clock.

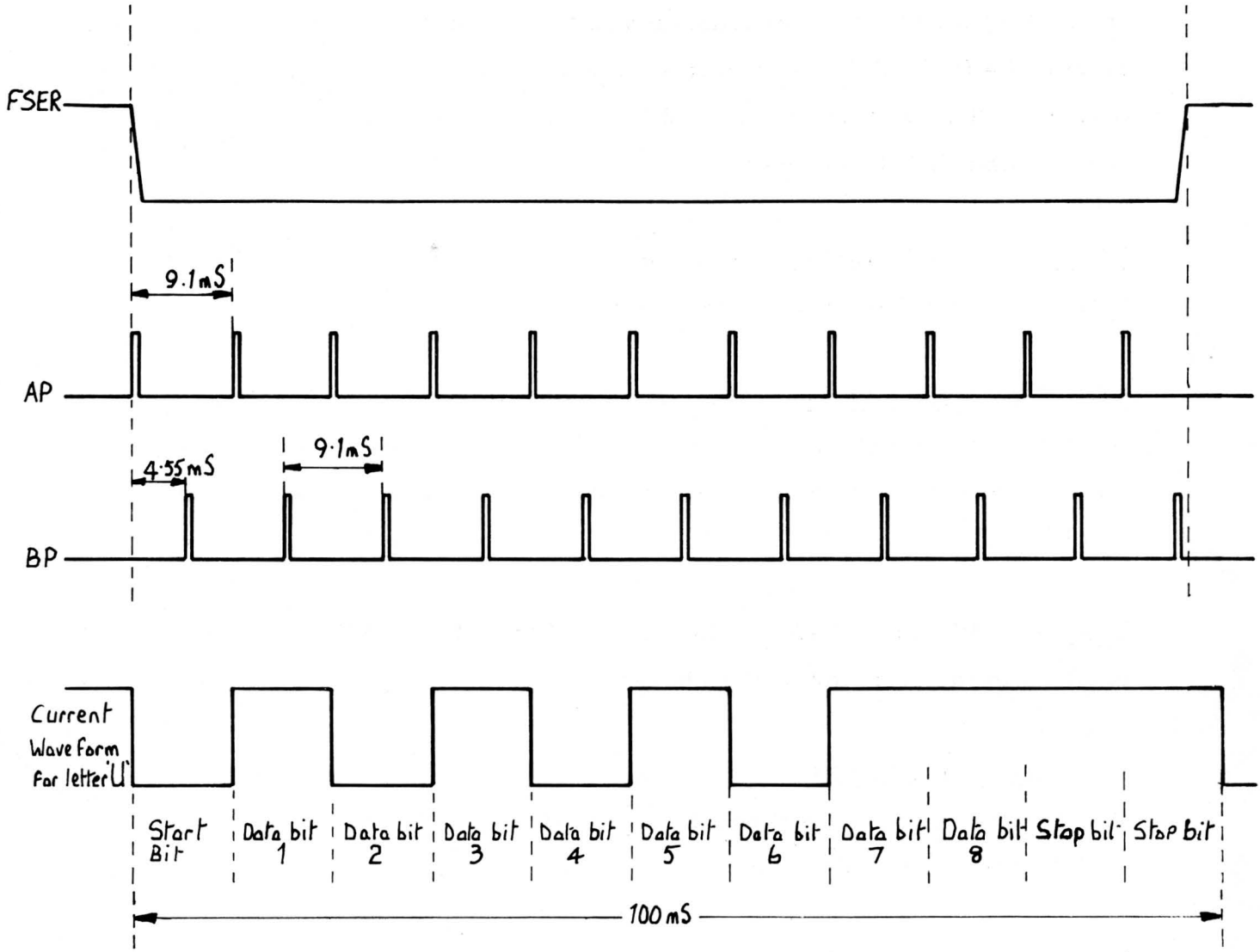
TIMING Figure 2.3 shows the timing of the AP and BP pulses in relation to the transfer of the character U.

2.8 SHIFT REGISTER

The register comprises three 4-bit modules F2, G2 and H2 (ref: B/10, C/9-10 and C/9) that can operate in either paralllel or one-bit shift modes. Only eleven bits of the register are used by the CU and figure 2.4 shows the inter-relationship of the three modules.

OPERATION The operation mode is determined by PE/. When this signal is present the register operates in the parallel mode. This mode is for all transfers between the register and the CPU. When PE/ is not present , the register operates in the one-bit shift mode the timing pulses from the CU clock providing synchronization with the ASR.

INR Command The register shifts one position during each BP pulse of the loading sequence (11 pulses in all). Input to the register is via B0 and the signal level LIN. Loading is initiated by the start pulse from the ASR which will be a low; then the eight character bits are



Notes:
1. The AP and BP pulses are both 400 nano-seconds wide.
2. Data bit 8 will always be high for any character.

Fiaure 2.3 CU Clock Timing

loaded followed by two stop pulses which will both be high. End of serialization is detected when the start pulse appears at Q10. This level is used via gates C4, G6 and D6 (ref: D and E/6-7) to reset FSER.

OTR Command The character on the BOU lines is loaded into register positions B3 to B9. The most significant bit of the character will always be a 1 so it is not transferred from the BOU lines but is inserted into register position B2 by the register itself. Position B10 is reset to represent the start bit and the other two positions (B0 and B1) are set to represent the two stop pulses. Output from the register to the serializer is from Q11 and as each pulse is sent to the ASR B0 is reset. End of serialization is detected when Q1 to Q10 have all been reset. These levels are used to produce level EMPTI1 which is used to reset FSER.

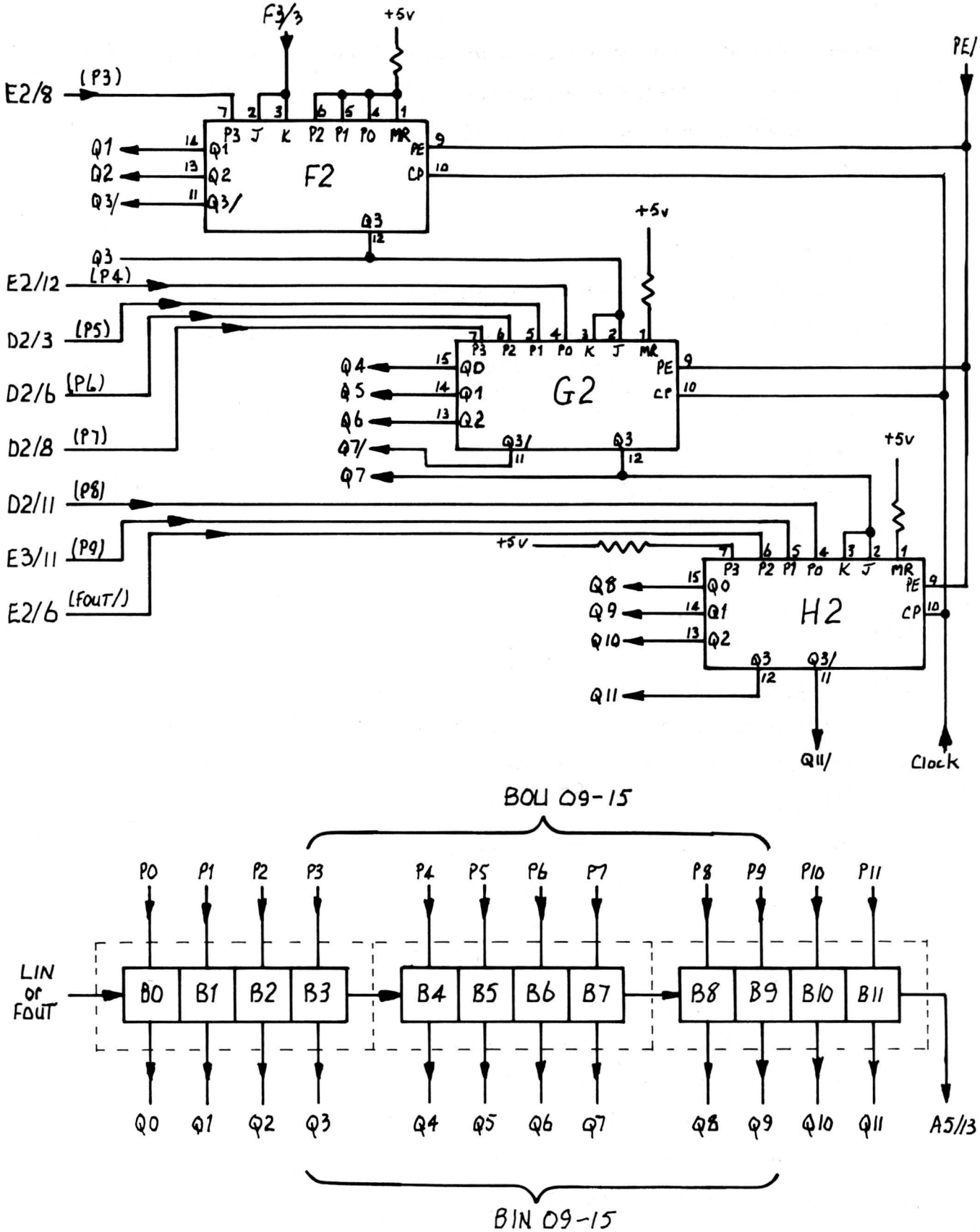
2.9 SERIALIZER

This circuit comprises T1, T2 and T3 (ref: D to G/7-8) and it is connected to the ASR via a single, twisted twin, cable. Data and control characters are sent along it as mark/space current wave form. A current of 20 milliamps represents a mark and a current of less than 3 milliamps represents a space. The relationship between the character U and the CU clock can be seen in figure 2.3.

2.10 STATUS RESPONSES

There are two types of status response one for the TST command and one for the SST command, and both use the same logic to send the response to the CPU. This logic is the G3 gates (ref: B and E/9) that load the BIN lines with the status. The same logic is also used during data transfers to the CPU to load BIN lines 14 and 15 with data.

TST The two responses to this command are inactive or busy. If the CU is inactive the response will be all lows on the BIN lines, if busy the CU will send a high on BIN 15.



Notes:

1. Q3 to Q9 also go to other gates as well as to the BIN lines.
2. Q8 and Q9 go to BIN 14 and 15 via the PARTBIN logic gates.

Figure 2.4 Shift Register

SST The response after a successful transfer will be all lows on the BIN lines. If a throughput error occurs during a transfer, the CU will send a high on BIN 14.

All other bits are insignificant for both types of command.

2.11 EXCHANGE CONTROL SIGNALS

These are the PIL/, BRL/ and EOR signals. The first two are used to ask the CPU to effect a data exchange, the last one tells the CU that the last character has been sent.

PIL/ This signal is active during the WST state and asks the CPU to send an SST command.

BRL/ This signal is active during the ECH state and asks the CPU to send either an INR or an OTR command. This signal is normally used only during multiplex exchanges, but when the ASR is used on the programmed channel the BRL/ and PIL/ signals are 'ored' together on the I/O bus.

EOR This signal is only used during multiplex exchanges to indicate to the CU that the last character has been either sent or accepted.

2.12 ASR TO CU CONNECTION

Both input and output data are transferred, between the CU and the ASR, via a pair of twisted wires. One of the wires is connected to pin A02 (logic level) and the other wire to pins A05 and A06 (ground) of an ELC0 connector socket. This socket is plugged onto the CU card and the other ends of the twisted pair are connected to the data input terminals of the ASR.

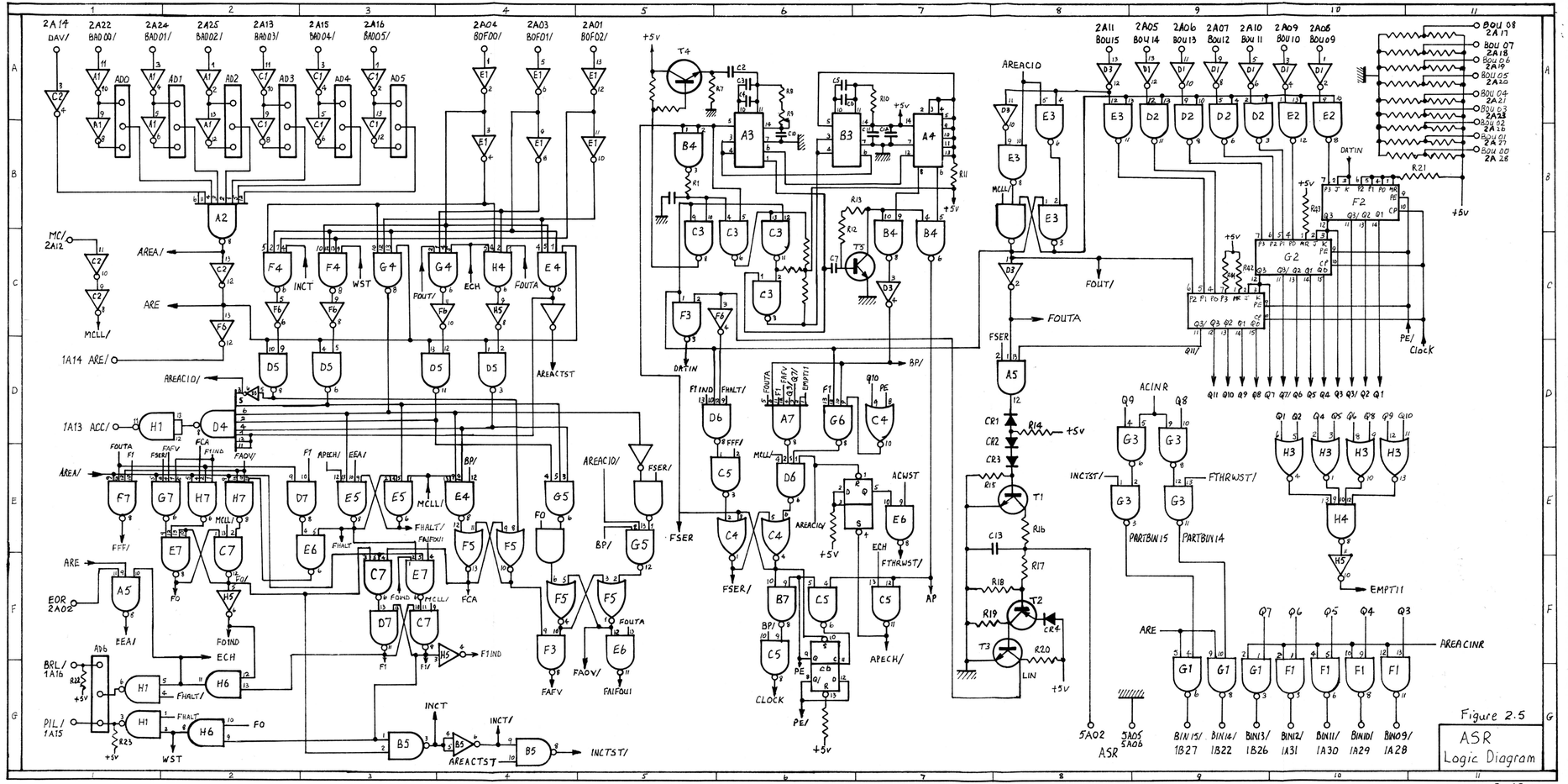


Figure 2.5
ASR
Logic Diagram

SECTION III

PUNCHED TAPE/CARD READER CONTROL UNIT

BRIEF DESCRIPTION

This control unit can be used to drive either a punched tape reader or a card reader. All the logic and special circuits are contained on one card and only one device can be connected to a card.

Figure 3.1 shows all the main logic blocks and data paths of the CU. The CU is connected to the CPU via the standard I/O bus. All I/O bus signals and their timing rules are detailed in Section I of this book. Connection between the CU and the device is via special circuits CSO and CSI and all these signal levels are active high.

When the CU is used with a tape reader, CSO will send the FWD (tape forward) and STOP (tape stop) commands to the device and CSI will interface the eight data channels, the strobe pulse and device status signals with the CU logic circuits.

When the CU is used with a card reader, the CSO signal FWD is used as the POC (pick one card) signal to the device; the stop signal is not used. The CSI circuits interface the twelve data channels, the strobe pulse and the device status signals to the CU logic circuits.

Operation of the CU is programmed by standard I/O instructions and data exchanges can be via either the programmed or multiplex channels depending upon the type of CPU.

At the end of this section is a fold-out drawing of the logic elements and special circuits that make up the CU. The grid reference points of this drawing are used in the following paragraphs to enable easy location of the relevant logic elements or special circuits. The CU functions in a similar way for both the tape and card reader so to avoid repetition, the following paragraphs apply to both devices unless otherwise stated.

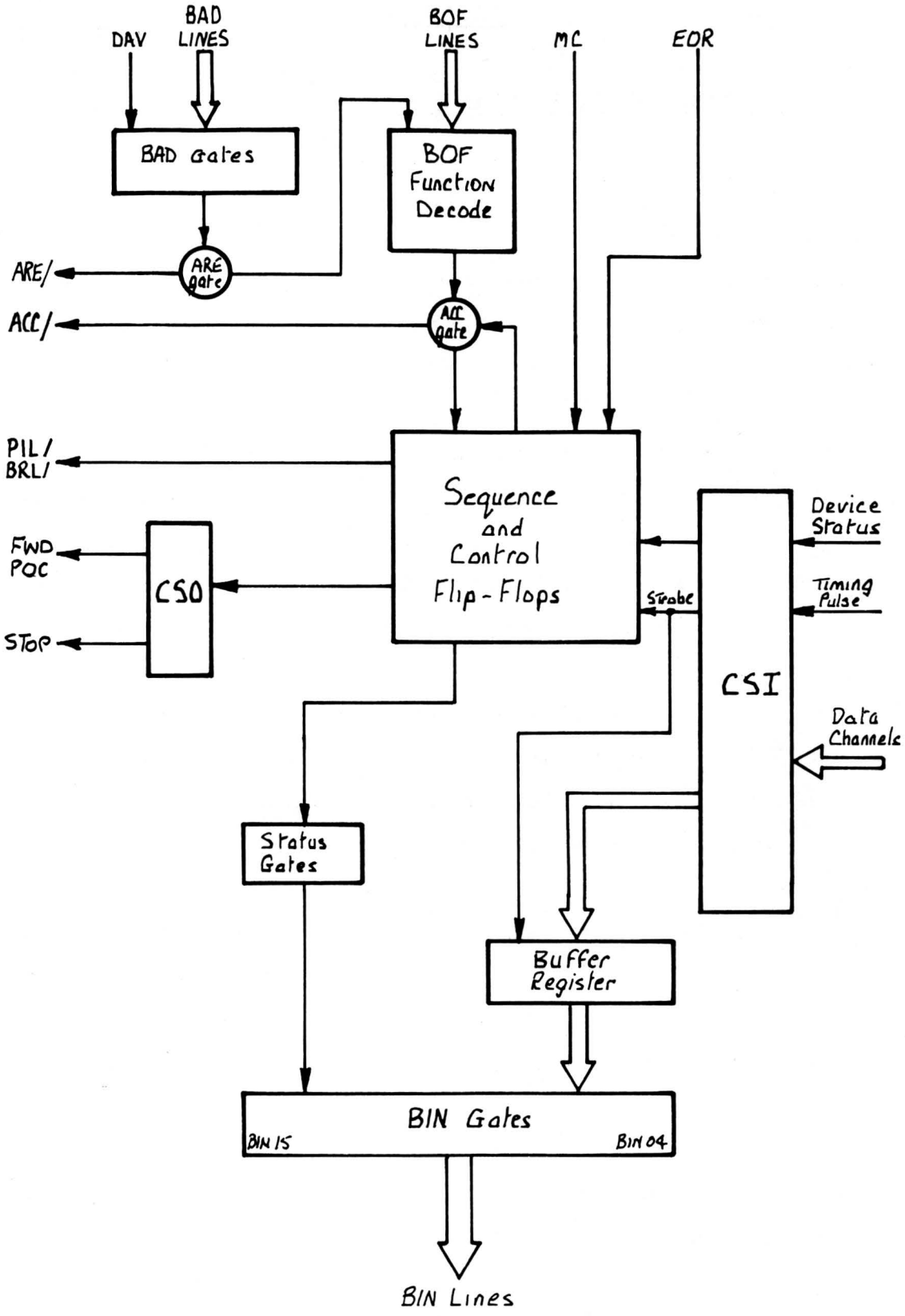


Figure 3.1 Block Diagram of Tape / Card Reader C.U.

3.1 ADDRESSING (BAD lines)

The CU can be wired to recognize any desired address using switch connectors AD00 to AD05 (ref: B/1-4). The outputs from the connectors together with the DAV/ signal, from the CPU, activate gate A2 (ref: C/2-3) producing AREA/ when the address is recognized. This signal is used to enable the BOF decoder, the interface sequencer and via the inverter B2 and gate G2 the ARE/ signal that is sent back to the CPU.

3.2 FUNCTION DECODING (BOF lines)

Data from the BOF lines is decoded by a 9301 module D1 (ref: B/4-5). The inputs to the module are validated by AREA/ and the outputs obey the following truth table:

INPUT	A2	A1	A0		OUTPUT
CIO	0	1	1	4/	START/
HIO	0	1	0	5/	ACHALT/
INR	1	0	*	2/3/	INRA/INRB/
SST	1	1	1	0/	SST
TST	1	1	0	1/	ACTST/

* can be either O or 1 depending on the function.

The outputs from the module are used to activate the control and sequence logic and in addition produces the ACC/ signal, via gates D2 and G1, that is sent back to the CPU.

3.3 INTERFACE SEQUENCER

This logic controls data transfers by switching the CU into the appropriate state. It is achieved by using a combination of the outputs from two flip-flops, F0 element A4 (ref: E/3) and F1 element A4 (ref: E/4).

INCT: is the inactive state and both F0 and F1 are reset. It is produced by either an SST command or the MCL/ signal. In this state the CU is waiting for a CIO start command to switch it into the execute state.

EXT: is the execute state and allows one character from the tape reader, or one column from the card reader to be read into the buffer register. It is entered when F0 is in the reset condition, and F1 has been set by either ACIO or ACINR. If the F0 flip-flop is set by gate C4 (ref: D-E/3), the CU will switch to exchange state; but if the F1 flip-flop is reset by gate C4 (ref: D-E/4) the CU will switch to the wait status state.

ECH: is the exchange state and is produced when both F0 and F1 are set. It allows the CU to ask the CPU for a data exchange by activating BRL/ via gate E1 (ref: E-F/2-3). The CPU will respond by sending an INR command which will activates gates C3 (ref: C/5) producing ACINR/. This signal is used to gate data on to the BIN lines and, via gate B3 (ref: E/5), to reset flip-flop F0 so that the CU can switch back to the EXT state to allow another character or column to be read from the device.

WST: is the wait status and is produced when F0 is in the set condition and F1 has been reset via gates D4 and C4 (ref: D/4-5). It allows the CU to send an interrupt to the CPU which responds with an SST command. This command causes the CU to send the status word back to the CPU, via the BIN lines, and resets flip-flop F0 so that the CU can switch back to the INCT state.

3.4 COMMAND FLIP-FLOPS

These are the FWD (ref: D/2) and FHALT (ref: F/6) flip-flops.

FWD This flip-flop remembers that a CIO start command has been accepted.

Set: by ACIO and in this condition will activate the CSO that sends the FWDPOC command to the device. When used to drive a card reader, this command is delayed by 10 milliseconds if a card has just been read.

Reset: by either FHALT, ACP or MCL. For the tape reader the reset condition activates the CSO that sends the STOP command to the device. This command is not used by the card reader.

FHALT This flip-flop remembers that either an HIO command has been accepted or that an error condition has been detected.

Set by either FHALTZ1 or ACHALTA. In this condition it resets FWD and inhibits any exchange request.

Reset by ACSST or MCL.

3.5 CONTROL FLIP-FLOPS

These are the FREAD (ref: D/3), the FTHR (ref: F/5) and FIL (ref: E/6) flip-flops.

FREAD This flip-flop remembers that the strobe signal STR has been received.

Set by STRB. In this condition it allows the CU to switch from the EXT to the ECH state.

Reset by either ACINR or CLEAR

FTHR This flip-flop remembers that a throughput error has been detected.

Set by STRA if the CU is in the ECH state.

Reset by either ACIO or MCL

FIL This flip-flop is used to indicate that the number of data characters is wrong when the CU is used with a card reader.

Set by FILZ1A if FHALT is not set when ACP is low.

Reset by either ACIO or MCL

3.6 SEQUENCE TIMING

Figure 3.2 shows the sequence timing of the CU during data transfers. The main differences between tape and card reader exchanges are in the timing of the STR pulse and in the resetting of the signal FWD.

TAPE READER SEQUENCE It can be seen from figure 3.2 that FWD is set by the CIO command and remains set until it is reset by FHALT. This means that once the tape has started to move forward, it will continue to move forward until FHALT causes it to stop; due to either an HIO command being accepted or an error condition being detected. Therefore the CPU must be programmed to accept the data characters in the buffer register before the next strobe pulse arrives at the CU, otherwise throughput errors will occur.

CARD READER SEQUENCE When the CU is used to drive a card reader, FWD is reset by ACP going high. The time between successive strobe pulses is even shorter, so again careful programming is needed to avoid throughput or incorrect length errors.

3.7 DEVICE INPUT SIGNALS

All these signals are active high and are interfaced with the CU logic via special circuits CSI (ref: B/6-11).

CP is the card present signal (ref: A/6) and it will remain high as long as the card covers the read station.

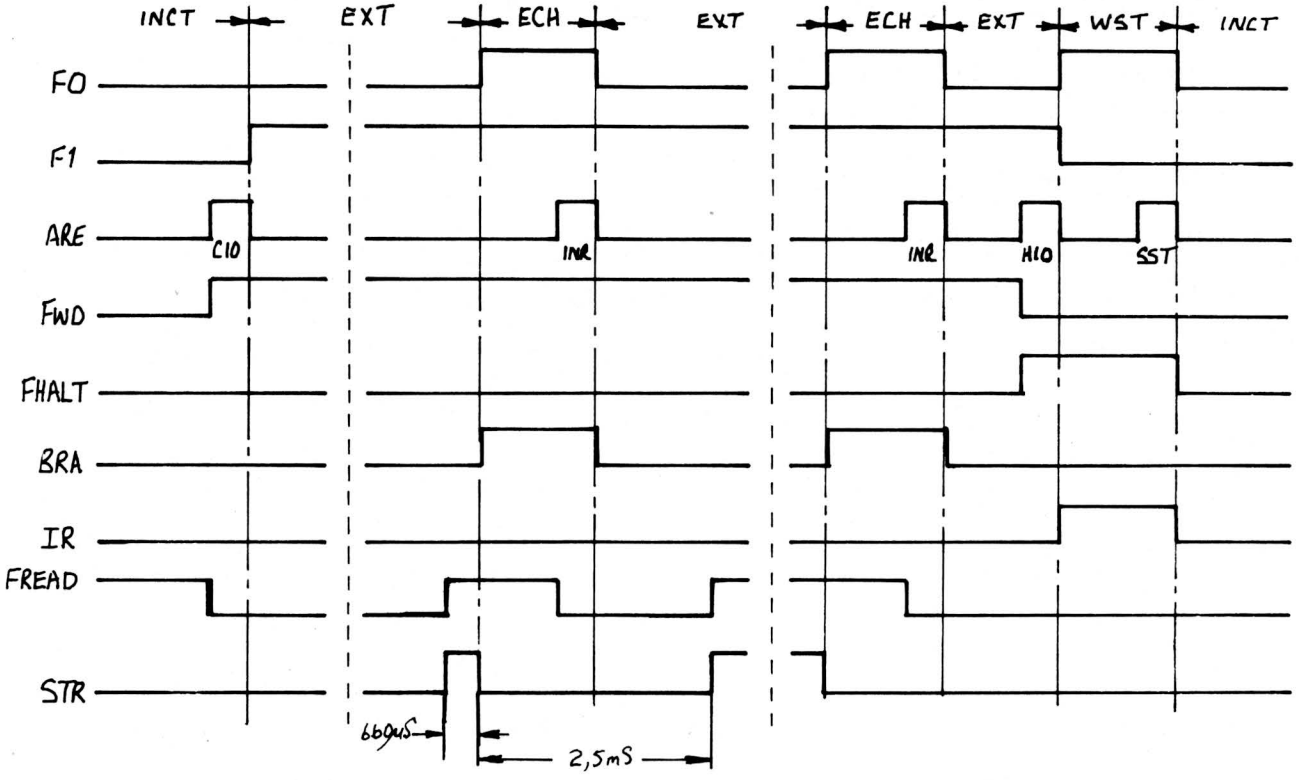
OPER is the card reader operable signal (ref: A/6).

LTLOPER is the load tape lever signal (ref: A/7).

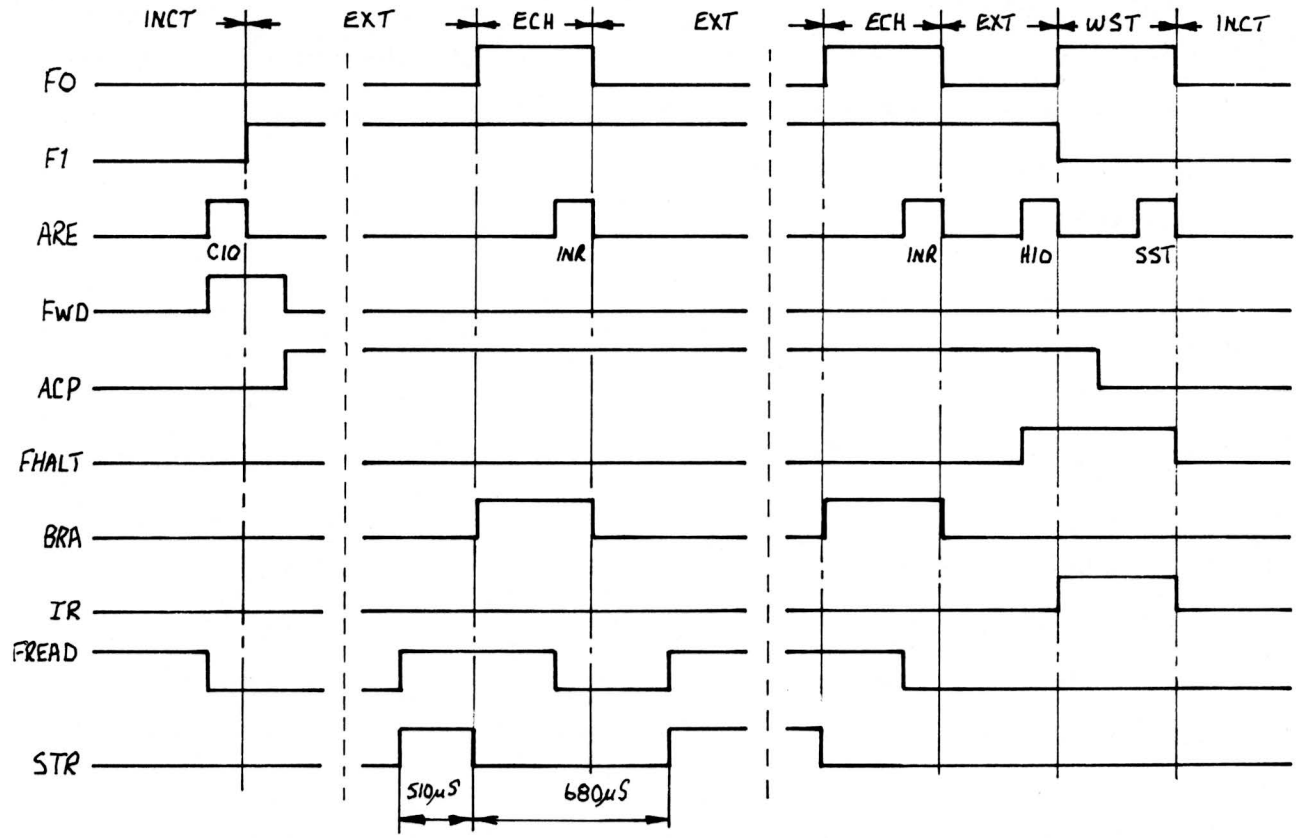
EOT is the end of tape signal (ref: A/7)

PKTBZS is either the SPKTB signal from the tape reader or the ZS signal from the card reader.

Timing for Tape Reader Exchanges



Timing for Card Reader Exchanges



Note: The section between the continuous dotted lines will be repeated as necessary until the end of the transfer.

Figure 3.2 Control Timing

DATA CHANNELS The remaining CSI signals are the data channels, eight from the tape reader and twelve from the card reader. These signals are loaded into the buffer registers.

3.8 BUFFER REGISTERS

These registers G4, F4 and H4 (ref: C-D/8-11) hold the data signals until they are transferred to the CPU by the INR command. The data is clocked into the register by strobe pulses STRA and STRB for the tape reader and by the STRA, STRB and STRC for the card reader. The outputs from the registers are input to one side of the BIN gates.

3.9 BIN GATES

The inputs to BIN gates 15, 14, 12 and 10 come from the buffer registers via logic that also provides status signals. All other BIN inputs come direct from the buffer. Data at these gates is enabled on to the BIN lines by ACINR for the first type of input and by ACINRA for the second type of input.

3.10 STATUS GATES

These gates are F2, F3 and E3 (ref: E/8-9) allow both the CU and the device status to be gated on to the BIN lines in response to either an TST or SST command from the CPU. The BIN lines used to indicate the status are:

BIN 15 a high on this line indicates that either the CU is busy or the device is not operable.

BIN 14 a high on this line indicates that a throughput error has occcured

BIN 12 a high on this line indicates that an incorrect length error has been detected

BIN 10 a high on this line indicates that end of tape has been detected.

All these status bits can be gated on to the BIN lines by ACSST, additionally BIN 15 can be gated by ACTST.

3.11 INTERRUPT SIGNALS

The gates which produce these signals are E1 and C2 (ref: E-F/2). When the CU is controlled by the programmed channel, both signals are 'ored' together on the I/O bus. The signals are:

PIL/ This signal is sent to the CPU when the CU enters the WST state and cancelled by the SST command.

BRL/ This signal is sent to the CPU when the CU enters the ECH state and is cancelled by the INR command.

3.12 OTHER SIGNALS

These are MC (ref: B/6) and EOR (ref: F/7)

MC_ This signal is sent from the CPU when either the CPU is switched ON or the operator pushes the MCL button on the control panel. It is used to reset the sequencer, command and control flip-flops of the CU.

EOR This signal is sent by the CPU during multiplex exchanges to indicate the end of the data exchange; it sets the FHALT flip-flop.

3.13 CU TO DEVICE CONNECTIONS

All connections are made via twisted pairs of wires. One of the wires is connected to ground - both at the CU and the device - and the other to the appropriate signal output. One end of the wires terminates at the Elco connector socket that plugs on to the 5A/B end of the CU card, the other end is connected to the appropriate device socket or card. The following table gives the connections for both the tape reader and card reader. In each case, the lefthand pin is the signal, the righthand pin is ground.

SIGNAL	CU SOCKET	TAPE READER SOCKET J1	CARD READER KAST/800 card
CH1 CH09	5A20/5B20	D/4	n/r
CH2 CH08	5A21/5B21	E/5	h/k
CH3 CH07	5A18/5B18	F/6	c/e
CH4 CH06	5A19/5B19	H/7	Y/a
CH5 CH05	5A16/5B16	J/8	U/W
CH6 CH04	5A17/5B17	K/9	P/S
CH7 CH03	5A14/5B14	L/10	K/M
CH8 CH02	5A15/5B15	M/11	E/H
CH01	5A24/5B24		A/C
CH00	5A25/5B25		t/v
CH11	5A22/5B22		x/z
CH12	5A23/5B23		BB/DD
EOT	5A13/5B13	aa/12	
PKTB ZS	5A12/5B12	N/12	F/J
LTLOPER	5A11/5B11	cc/25	
OPER	5A07/5B07		L/N
CP	5A10/5B10		B/D
FWD POC	5A08/5B08	18/12	R/T
STOP	5A09/5B09	20/12	

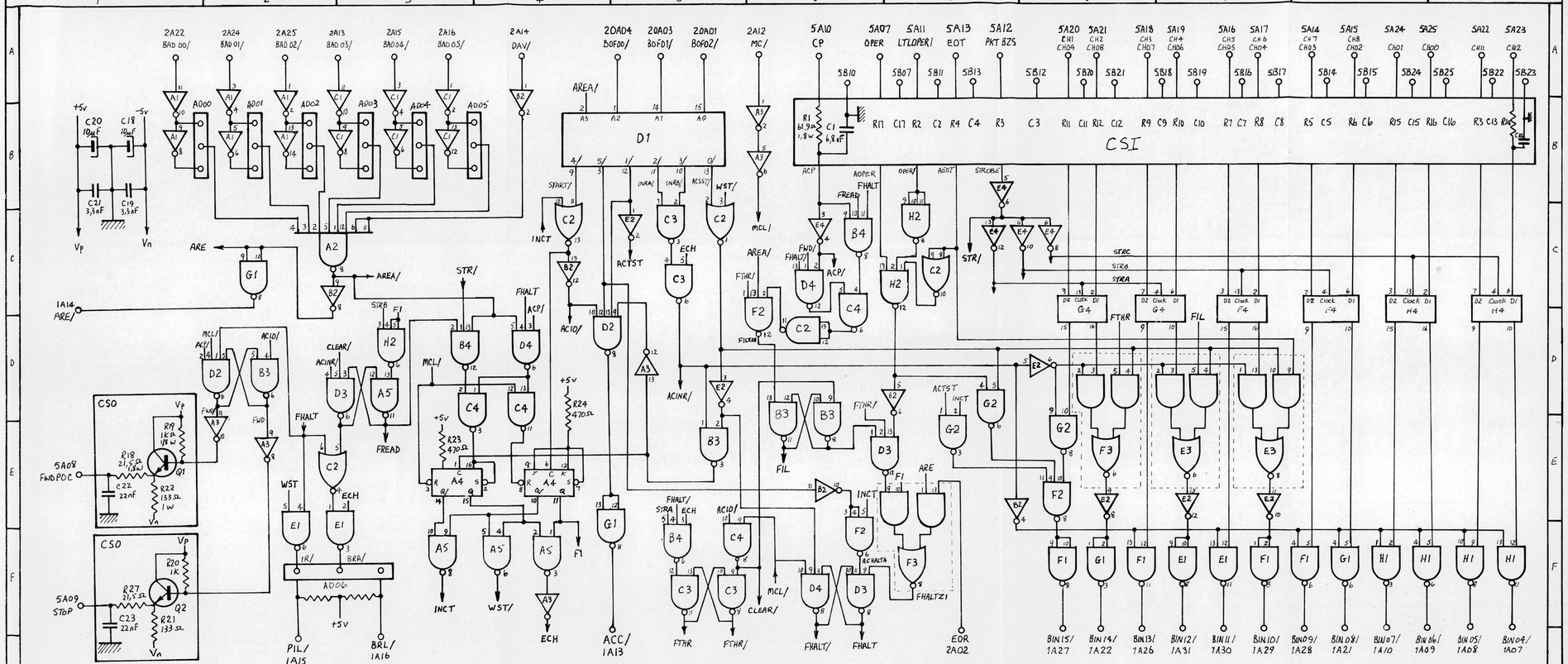


Figure 3.3

Tape/Card Reader Logic Diagram

SECTION IV

TAPE PUNCH CONTROL UNIT

BRIEF DESCRIPTION

A block diagram of the tape punch CU is shown in Figure 4.1. All the logic and special circuits are contained on one card that is plugged into an I/O bus socket and only one punch can be connected to a card. The special circuits CSI and CSO are used to interface the device to the CU logic circuits. CSI is used for the input signals from the device and CSO is used for the data channels and the command signals to the device. All the special circuit levels are active high. Operation of the CU is controlled by standard I/O instructions and status signals from the device.

The logic and special circuit diagram, which will be found at the end of this section, should be used when reading the following paragraphs. It has grid reference points that are referred to in the text to enable easy location of the circuit elements being described.

4.1 ADDRESSING (BAD Lines)

The address of the CU can be wired to recognize any desired address using switch connectors AD00 to AD05 (ref: A-B/1-3).

The outputs from these connectors together with the DAV signal from the CPU are gated via element B2 (ref: C/2) to produce the AREA/signal that is used to enable the BOF decoder and the sequencer. It is also used, via element H1 (ref: D/1) to produce the ARE signal that is sent back to the CPU when the address is recognized.

4.2 FUNCTION DECODING (BOF Lines)

The command from the BOF lines is input to element D1 (ref: A-B/4-5) that decodes the function the CU is asked to perform. If the command is accepted, the ACC signal is sent back to the CPU via H2 and H1 (ref: E-F/4) and the active output level is used to enable other logic elements of the CU. Which element it will be can be seen by refering to the following truth table.

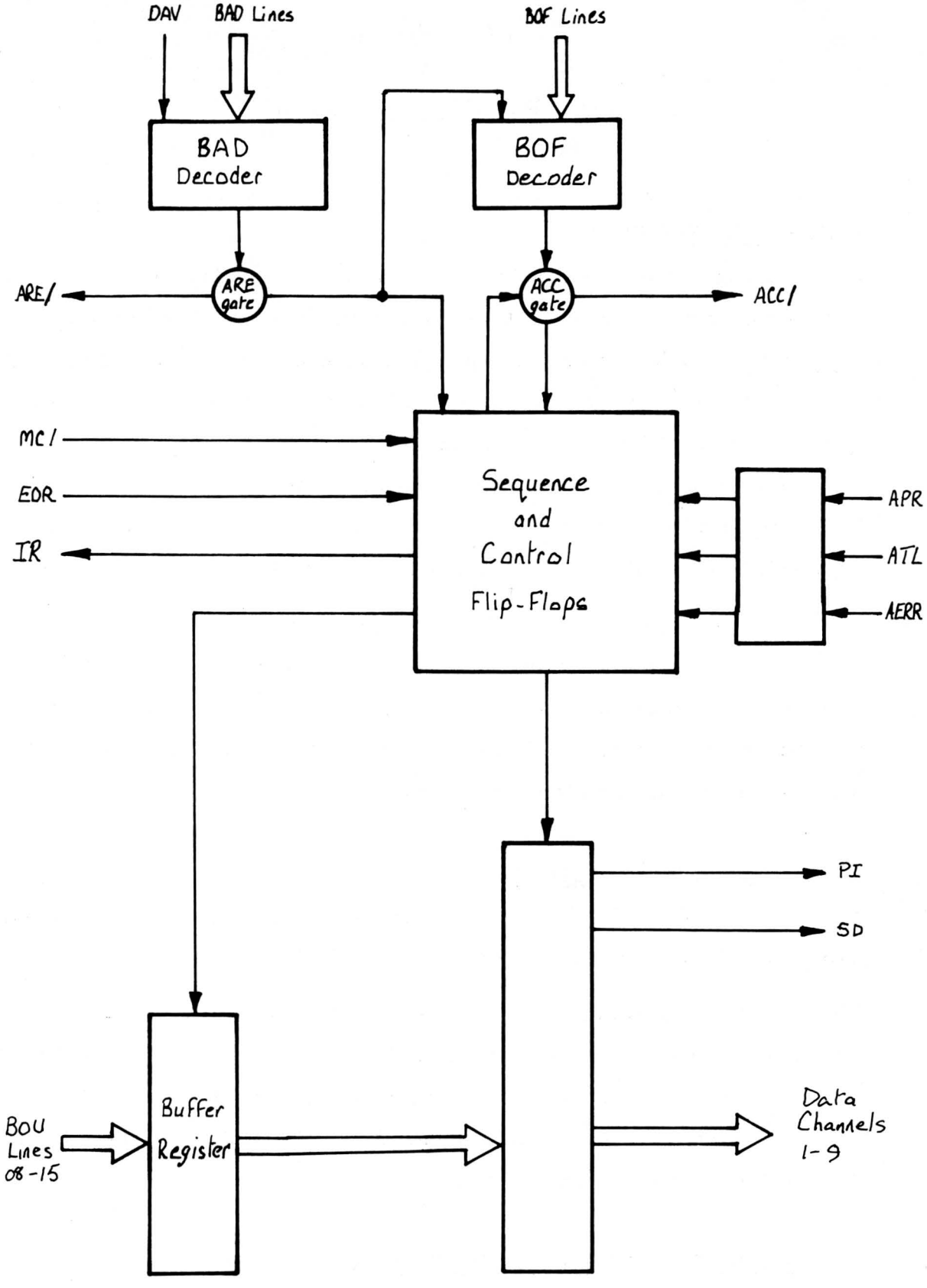


Figure 4.1 Block Diagram of Tape Punch C.U.

A2	A1	A0	Output	(Pin N°.)
0	0	X	OTR	4 + 5
0	1	0	CIO Stop	3
0	1	0	CIO Start	9
1	1	0	TST	12
1	1	1	SST	13

The CIO Stop and the TST commands are always accepted; but before the other commands can be accepted, the CU must be in the appropriate state.

4.3 INTERFACE SEQUENCER

The sequencer uses two flip-flops F0 (ref: E-F/2) and F1 (ref: E-F/3) to switch the CU into one of the four states.

INCT Both F0 and F1 are reset. It is switched into this state either by MC or the trailing edge of an SST command. In this state the CU is waiting for an I/O command.

ECH Both F0 and F1 are set. It is switched into this state by either the trailing edge of the CIO start command or when signal PR goes high at the end of the execute state. In this state the CU askes the CPU for a data exchange and loads the buffer register with data.

EXT F1 is set and F0 has been reset by the trailing edge of the OTR command. In this state the punch instruction is sent to the device and data holes are punched into the tape.

WST F0 is set and F1 is reset by the level FHALT. This will occur when either a CIO stop command is received or an error has been detected. In this state the CU sends an interrupt to the CPU and waits for an SST command. The leading edge of the SST command will reset FHALT and the trailing edge of the command will switch the CU into the INCT state.

4.4 CONTROL FLIP-FLOPS

These are FPI (ref: D-E/3-4) and FHALT (ref: G/6).

FPI This flip-flop remembers that a punch instruction must be performed. One of the outputs from this flip-flop is used via element G3 (ref: E/3) to send the punch instruction to the device.

Set: When the leading edge of the OTR command produces ACOTR via gates E2 and D2 (ref: C/5).

Reset: by either PR, ACSST or MCL

FHALT This flip-flop indicates that an exchange must be ended because either a CIO stop command has been accepted or an error condition has been detected.

Set: by either ACHALT or LTZ1

Reset: by either ACSST or MCL.

4.5 SEQUENCE AND CONTROL TIMING

Figure 4.2 shows the timing of the sequencer and control flip-flops. The time taken to complete one punch cycle may vary slightly from the minimum time shown in the diagram up to a maximum time of 13.3 milliseconds. This variation is dependant up on the time taken by the punch to execute the PI instruction.

4.6 BUFFER REGISTER

This register (ref: B/6-8) comprises two 4-bit latches. Data on BOU lines 08 to 15 is loaded into the register by the clock pulse given by ACOTR. The outputs of the register are connected to the punch data channels via special circuits CSO (ref: C-D/9).

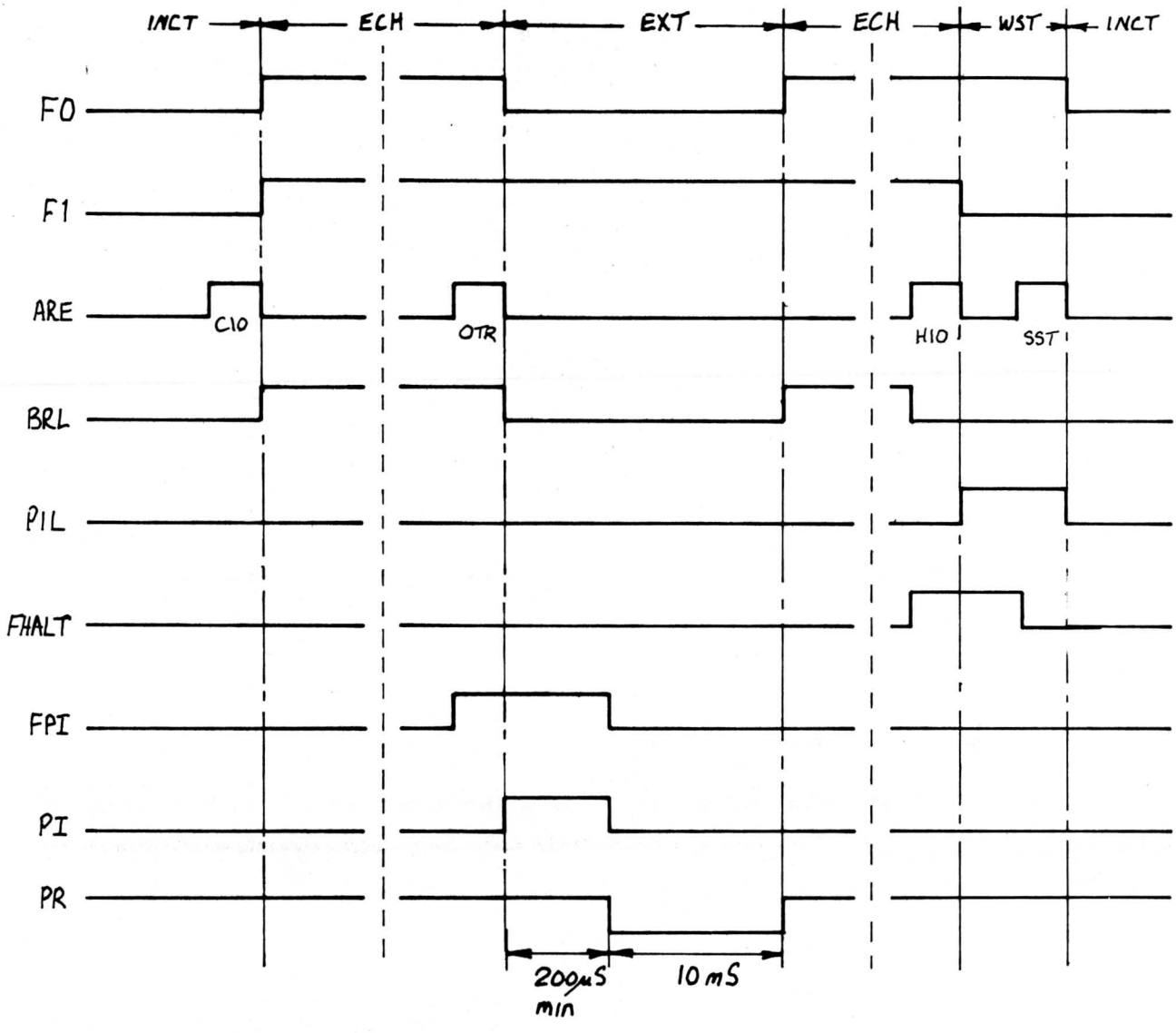
4.7 INTERRUPT SIGNALS

These are BRL (ref: G/4) and PIL (ref: G/3).

BRL This signal is sent to the CPU when the CU switches into the ECH state. It is cancelled by the trailing edge of the OTR command or by FHALT.

PIL This signal is sent to the CPU when the CU switches to the WST state. It is cancelled by the trailing edge of the SST command.

When the CU is controlled by the programmed channel, the BRL and PIL signals are 'ored' together on the I/O bus.



The section between the dotted lines will be repeated as necessary until transfer is ended.

Figure 4.2 Sequence and Control Timing

4.8 PUNCH INPUT SIGNALS

These signals are APR, ATL, and AERR and they are interfaced to the CU logic via special circuits CSI (ref: E/9).

APR Is the punch ready signal. It goes low when data has been stored in the device register and goes high when punching is completed.

ATL Is the tape low signal. It is sent by the punch detects that a new roll of tape is needed.

AERR Is the error signal. It is sent by the punch when either the tape becomes too tight or has broken.

4.9 STATUS GATES

These are gates G1 and E1 (ref: F-G/4-5). The outputs from the gates are sent to the CPU in response to either an SST or a TST command.

BIN15 A high is output to the CPU on this line if either the CU is busy or the punch is inoperable due to an error condition.

BIN10 A high is output to the CPU if the tape low signal has been sent from the punch.

4.10 OTHER SIGNALS

These are SD (ref: D/9), EOR (ref: G/6) and MC (ref: D/1).

SD Is the stepping direction signal to the punch. It should always be low to indicate forward.

EOR This signal is sent by the CPU during multiplex exchanges to indicate the end of a data exchange; it sets the FHALT flip-flop.

MC This signal is sent from the CPU when either the CPU is switched ON or the operator pushes the MCL button on the control panel. It is used to reset the sequencer and control flip-flops.

4.11 CU TO PUNCH CONNECTIONS

All connections are via twisted pairs of wires. One of the wires is connected to ground - both at the CU and the punch - and the other wire is connected to the appropriate signal output. One end of the wires terminates at the Elco connector socket that plugs on to the 5 A/B end of the CU card, the other end is connected to plug P1 of the punch.

In the following table of connections the lefthand pin is the signal, the righthand pin is ground.

SIGNAL	CU SOCKET	PUNCH PLUG
ACH1	5A01/5B01	1/25
ACH2	5A05/5B05	2/25
ACH3	5A06/5B06	3/25
ACH4	5A04/5B04	4/25
ACH5	5A07/5B07	5/25
ACH6	5A09/5B09	6/25
ACH7	5A10/5B10	7/25
ACH8	5A08/5B08	8/25
ACH9	5A03/5B03	9/25
API	5A02/5B02	11/25
SD	5A11/5B11	10/25
APR	5A21/5B21	12/25
ATL	5A12/5B12	21/25
AERR	5A13/5B13	20/25

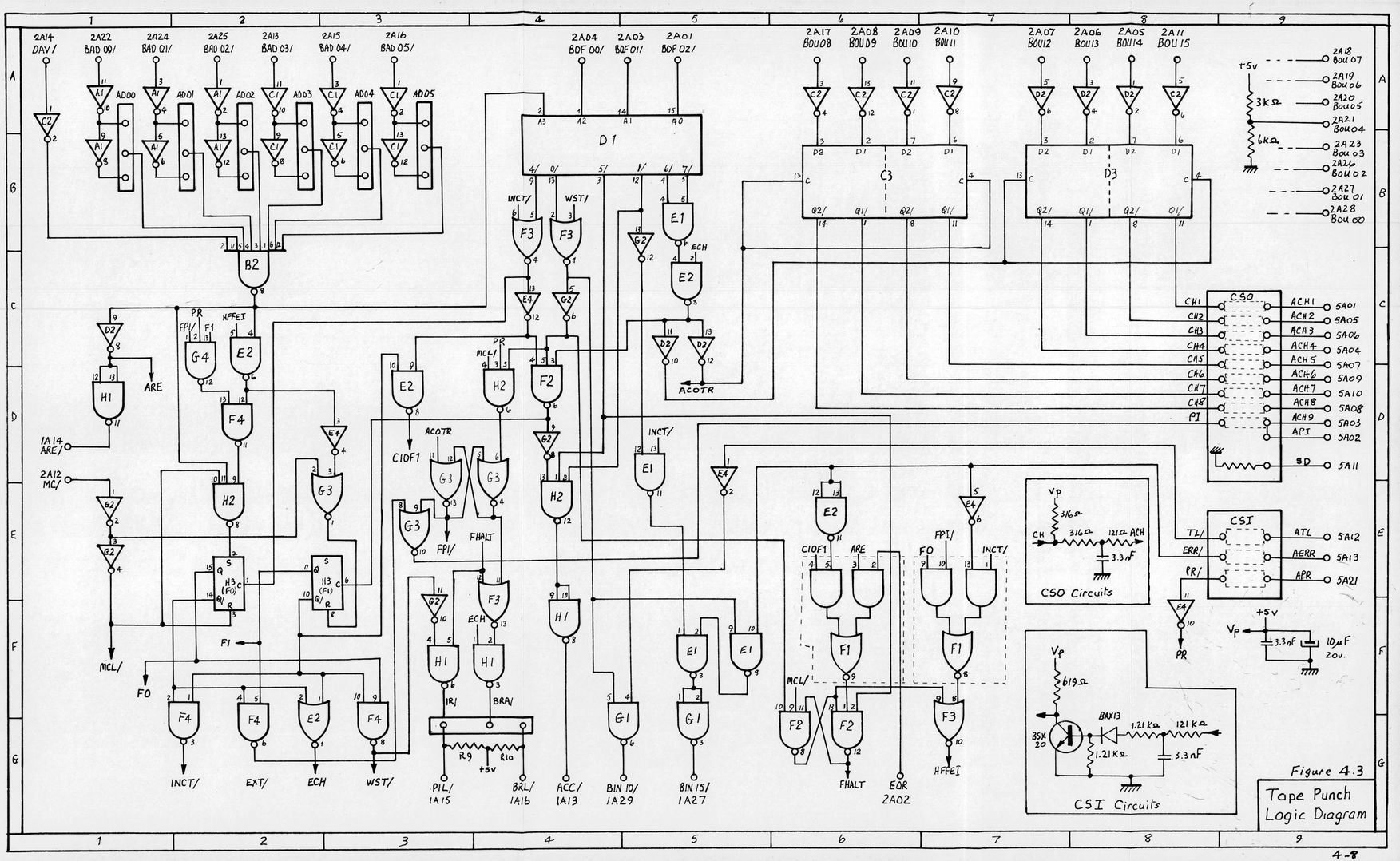


Figure 4.3
Tape Punch Logic Diagram

SECTION V

DIGITAL INPUT/OUTPUT SYSTEM (DIOS)

5.1 BRIEF DESCRIPTION

The Digital Input/Output System provides the interface and control logic required to transfer information between digital peripheral equipment and the programmed channel of an 800 Series computer. Some typical examples of DIOS configurations are shown in Figure 5.1 below.

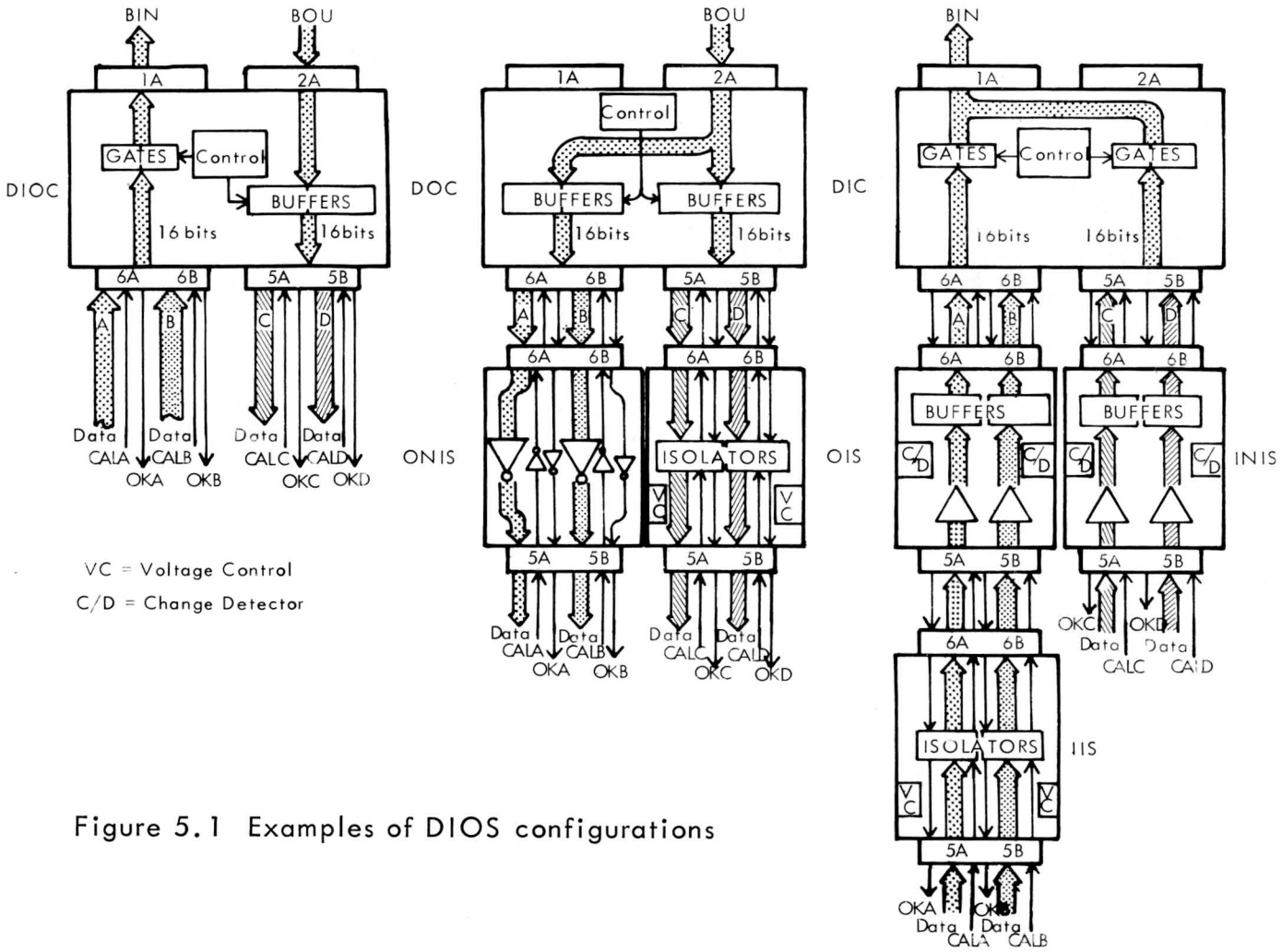


Figure 5.1 Examples of DIOS configurations

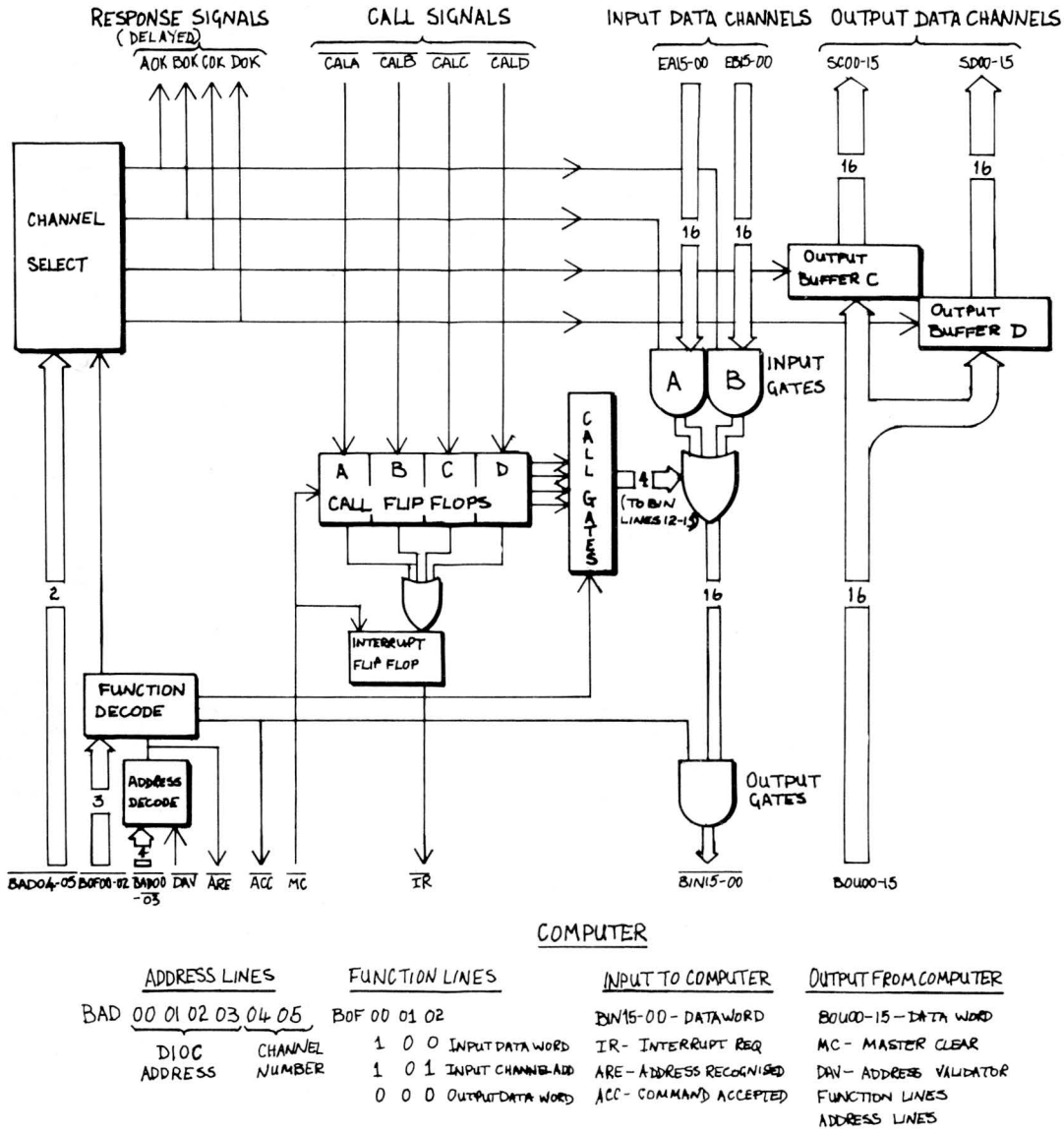


Figure 5.2 Block Diagram of DIOC

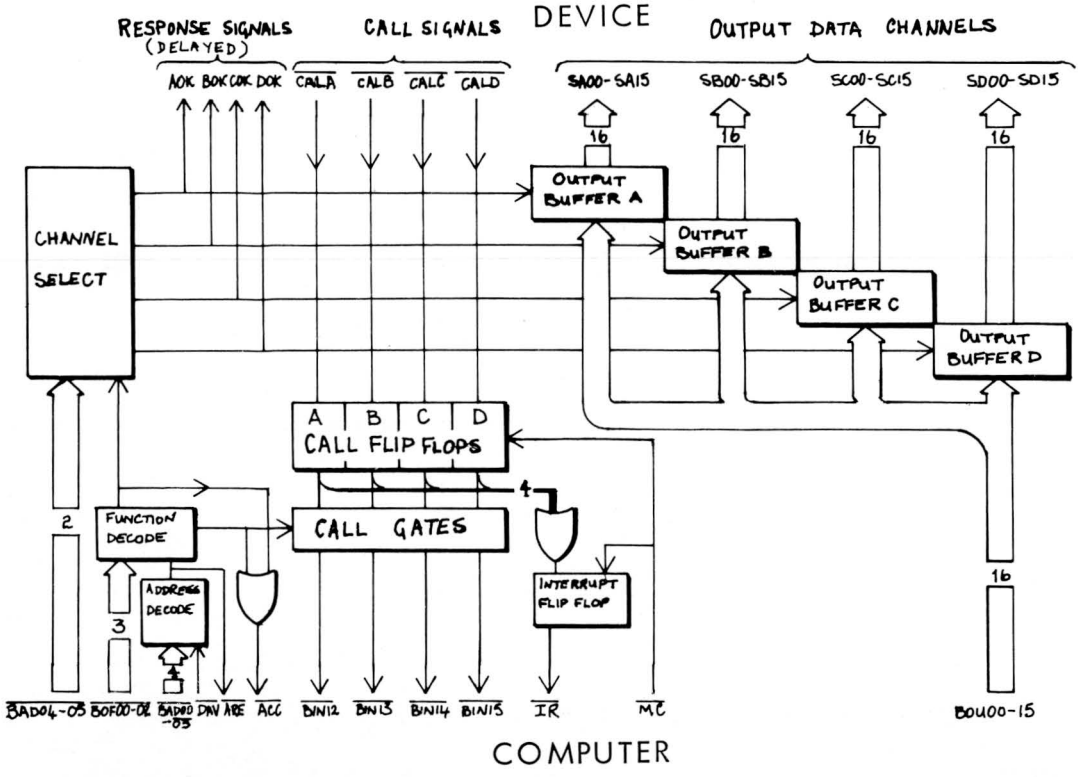


Figure 5.3 Block Diagram OF DOC

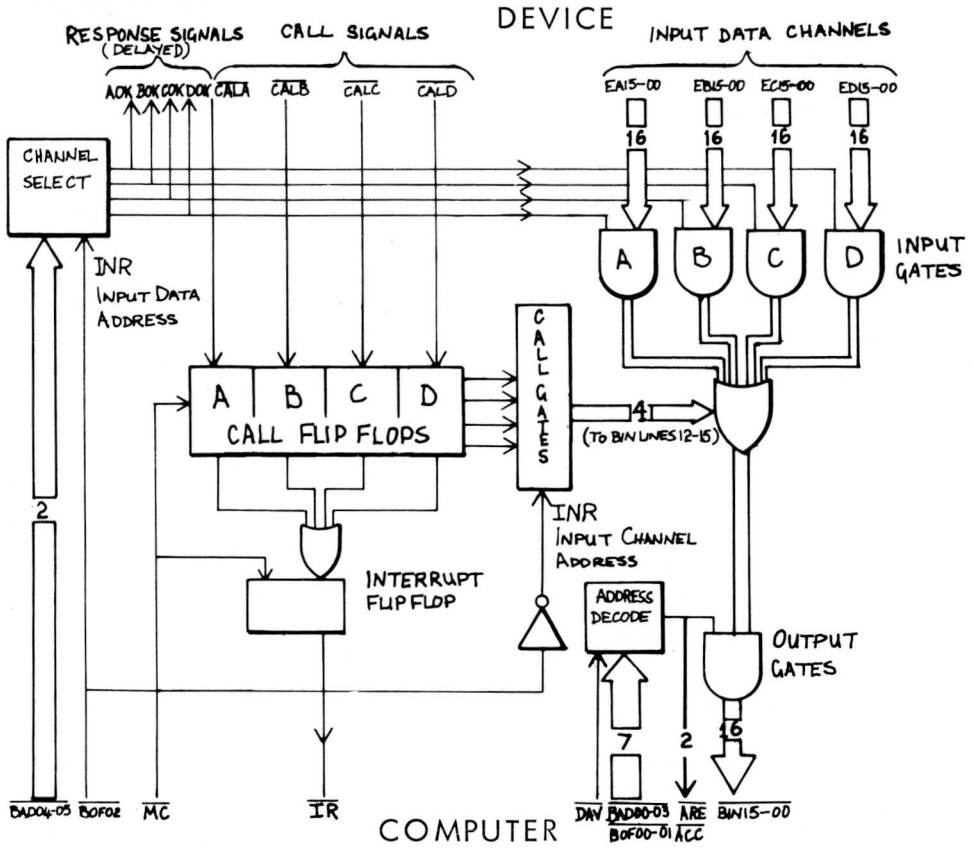


Figure 5.4 Block Diagram of DIC

The DIOS may be supplied in any of the following forms to suit the requirements of the customer:

(i) Digital Input Controller (DIC): to provide the interface buffering and control logic for four 16-bit input channels (A, B, C and D) see block diagram Figure 5.4. The DIC is contained on one card.

(ii) Digital Output Controller (DOC): to provide the interface buffering and control logic for four 16-bit output channels, see block diagram Figure 5.3 The DOC is contained on one card.

(iii) Digital Input/Output Controller (DIOC) to provide the interface and control logic for two input (A and B) and two output (C and D) 16-bit channels, see block diagram Figure 5.2 The DIOC is contained on one card.

In addition to the basic cards described above optional cards may be used to provide:

(a) Buffering of the incoming data (INIS) - there are no storage facilities in either the DIC or DIOC for incoming lines.

(b) Change of state detection (INIS) - to inform the computer when a change of data on the incoming data lines occurs.

(c) Level adaptation (INIS, ONIS) - to match the interface logic levels with those of the digital equipment.

(d) Galvanic isolation (IIS, OIS) - to completely isolate, electrically, the external digital equipment from the system.

5.2 ADDRESSING

The address of the DIOS may be selected using straps which connect the address decode gate (shown on the schematic diagrams) in the DIOS to BAD lines 02-05. The address part of the instructions are checked when a validity signal DAV is received from the computer. If the address is accepted the signal ARE is returned to the computer and function decoding is enabled. If a data transfer function is requested the channel address is specified on BAD lines 00 and 01 as follows and decoded by the

Channel Select gates once the controller address has been accepted.

BAD	00	01	
	0	0	Channel A
	0	1	Channel B
	1	0	Channel C
	1	1	Channel D

5.3 FUNCTION DECODING

The function of instruction is determined by BOF lines 00-02. The functions recognized by each of the DIOS units are as follows:

BOF Lines			Function	Recognized by
00	01	02		
1	0	1	Input Word Address (INR)	All units
1	0	0	Input Data Word (INR)	DIC and DIOC
0	0	0	Output Data Word (OTR)	DOC and DIOC

When a function code is accepted the signal ACC is returned to the computer.

5.4 SEQUENCE OF OPERATION

The following description is applicable to all the DIOS units except where otherwise stated. Data transfer between the device and the computer may be initiated by either:

(i) Control from the device

Where the transfer is initiated by the device, a CAL/signal of between 0.5 μs and 2.0 μs must be generated and sent to the DIOS to request each 16-bit word transfer. The 'call' is stored in the DIOS by the Call flip-flops, one for each channel, and an interrupt (IR/) is sent to the computer. The computer responds to the interrupt with an Input Word Address INR instruction. If this instruction is accepted the Interrupt flip-flop in the DIOS is reset

and the Call and Output gates enabled to place the contents of the Call flip-flop on input BIN 15-12. Output gates are not required in the DOC and the CAL information is placed directly onto the input lines via the Call gates. The call information is examined in the computer to determine which channel has demanded the transfer and whether an input or output transfer is required; the latter is defined by the type of unit or in the case of the DIOC the channel address (A and B are input channels and C and D are output channels). A second instruction is then sent to the DIOS to enable the data transfer.

(ii) Input Data Transfers

For incoming transfers an Input Data Word INR instruction is sent to the DIC or DIOC with the controllers address and channel number specified as described previously. If the instruction is accepted the Output gates and Channel Select gates are enabled. The Channel Select gate returns a response signal (AOK, BOK, COK or DOK) to the device which initiated the transfer, resets the Call flip-flop for that channel and enables the appropriate Input gates to transfer the data onto the BIN lines. The response signals to the device are delayed between 2 and 20 μs, see paragraph 5.7.

(iii) Output Data Transfers

For output data transfers an Output Data Word OTR is sent to the DOC or DIOC with the DIOC with the address and channel number specified as described previously. The instruction is handled in much the same way as the INR described above but with the information on the computer output lines (BOU) being clocked into the appropriate Channel Buffer instead of the Input gates being enabled.

(iv) Software Control

Data may be transferred to and from a digital device under software control without a CAL signal from the device. Input Data Word instructions are used to sample the input lines from the device

at intervals controlled by the software, see (ii) above. Output data is loaded into the buffers in the DIOS by Output Data Word OTR instructions. A response signal (AOK, BOK, COK, or DOK) is sent to the device when the buffer is loaded. The data remains in the Output buffer until over-written by new data from the computer.

5.5 TIMING

The timing of data transfers through the DIOS is dependant on the I/O bus timing (see Section 1 Figure 1.2). Since no buffering is provided for the standard DIOS input channels, data could be lost if CAL interrupts are not serviced promptly.

5.6 RESETTING

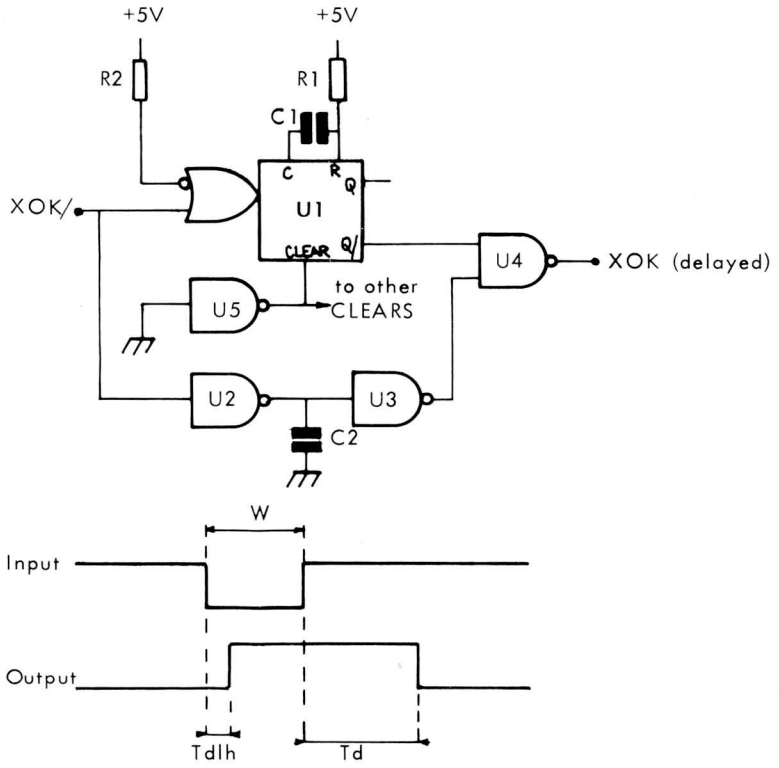
The CALL flip-flops can be either reset together by a MC (Master Clear) signal from the computer or separately when the computer responds to a CAL on that channel. The INTERRUPT flip-flop is also reset by a MC signal or when the computer responds to a CAL.

5.7 DIOS to DEVICE INTERFACE

Connections between the DIOS and the digital devices are made using twisted pair wires between ELCO connectors. The DIOS interface in its standard form, without optional circuits, will match with normal TTL or DTL digital devices. The connector pin connections are :

Signal	Connector and Pin Number				Signal	Connector and Pin Number (cont)			
	Channel A	B	C	D		Channel A	B	C	D
00	6A25	6B25	5A07	5B07	10	6A12	6B12	5A20	5B20
01	6A24	6B24	5A08	5B08	11	6A11	6B11	5A21	5B21
02	6A23	6B23	5A09	5B09	12	6A10	6B10	5A22	5B25
03	6A22	6B22	5A10	5B10	13	6A09	6B09	5A23	5B24
04	6A21	6B21	5A11	5B11	14	6A08	6B08	5A24	5B23
05	6A20	6B20	5A12	5B12	15	6A07	6B07	5A25	5B22
06	6A19	6B19	5A13	5B13	CAL	6A16	6A05	5A16	5A05
07	6A18	6B18	5A14	5B14	OK	6B16	6B05	6B16	5B05
08	6A14	6B14	5A18	5B18	Ground	6A01	6B01	5A01	5B01
09	6A13	6B13	5A19	5B19		6A17	6B17	5A17	5B17

5.8 SPECIAL DELAY CIRCUIT



Timing measurements with the input driven by a TTL gate and the output open:

TdlH = 45ns typical

Td = 19.6 μs typical

W = undefined

The circuit shown above is used to delay the DIOS response (OK) signals. The delay of the response signal can be adjusted, within the limits 1μs - 20μs, by changing the value of R1 or C1.

Circuit characteristics:

Input Low	0.2V - Fan In	2
Input High	3.4V - Fan In	2
Output Low	0.2V - Fan Out	10
Output High	3.2V - Fan Out	10

Power is supplied from the processor + 5V ± 5%

The delay provided by the circuit may be adjusted by changing resistor R1 as shown in the table below:

R1	Td
17.8K	19.6 μs
8.25K	9.1 μs
1.78K	1.9 μs

or by changing capacitor C1 with R1 = 17.8K as follows:

C1	Td
3.3nF	19.6 μs
1.8nF	10 μs
820pF	5 μs
330pF	2 μs

Components:

R1	1 X	17.8K	1/8W (typical)
R2	1 X	1K	1/8W
C1	1 X	3.3nF	Ceramic plate
C2	1 X	330pF	Ceramic plate
U1	1/2	U7B 960259X	
U2	1/6	7404	
U3	1/6	7404	
U4	1/4	7400	
U5	1/6	7404	

Details of individual components and their physical locations are supplied with the appropriate DIOS logic diagram.

5.9 EXTENDED DIOS

Special circuits may be used to extend the facilities provided by the standard DIOS and adapt the DIOS/Device interface to match specific customer requirements.

The special circuits available are:

INIS - Input adaptor Not ISolated

ONIS - Output adaptor Not ISolated

IIS - Input adaptor ISolated

OIS - Output adaptor ISolated

5.10 SPECIAL CIRCUIT CARD-INIS

The INIS card may be used with either a DIC or DIOC to buffer and provide change of stage detection circuits for two 16-bit input channels. The INIS card also provides logic levels changers to match the control and data logic levels of the device to those of the DIOS. The INIS card may be supplied in either of two forms:

(i) The INIS LT (two channels),to match symetrical input logic levels to those of the DIOS (high input +6V, low input -6V).

(ii) The INIS HT (two channels), to match asymetric input logic levels to those of the DIOS (high input +15V, low input 0V).

The level changing is achieved by receiver circuits, one for each of the incoming lines. If any of these functions are not required they may be strapped out on the INIS card itself.

5.11 Receiving Circuits

The Data and Call signals from the device are matched to the logic levels of the DIOS by the receiving circuits. With the low threshold option input signals can be in the range:

High = +2.0V to +48V

Low = -48V to +0.4V

With the high threshold option input signals can be in the range:

High = 7.5V to 48V

Low = -48V to 4.5V

In both cases Isink at low level 1.8mA

Iload at high level 1.0uA

The length of the cable connecting the INIS card to the device sets a minimum value on these input voltages as follows:

Distance	Connection	Noise Margin	ONIS	High	Low
15M	single wires	3V	LT	+5V	-2.2V
			HT	+10.5V	+1.5V
15 to 50	twisted wires	4V	LT	+6V	-3.2V
			HT	+11.5V	+0.5V
50M	twisted	6V			

5.12 Driver Circuits

Driver circuits are used to amplify the output from the receiver circuits sufficiently to drive the Buffer flip-flops and the change of state detection logic. The driver circuits have the following characteristics:

Low Input 0.2V typ Output 0.2V
with Isink = 50mA

High Input 3.3V typ Output 47V
V sup = 48V
Iload = 0.1mA

5.13 Change of State Logic

Data on the Input lines may be clocked into the Buffer flip-flops by either a response signal (XOK) from the computer or a CAL signal from the device. If the digital device cannot supply CAL signals the change of state detection logic in the INIS may be used to clock data into the buffer. The change of state logic triggers a monostable when the data on the incoming lines changes, the 1 μs ground pulse produced generates a CAL signal for the DIOS and clocks the data into the buffer.

5.14 Transmitting Circuits

The transmitting circuits provide the level adaptation for the response signals (XOK). The power for the transmitting circuits is supplied by the user and can be adjusted to give output voltages within the range:

High = 2.4V to 48V at 0.1mA

Low = Less than 0.4V max I = 50mA

The length of the cable connecting the INIS card to the device sets a minimum value on these output voltages as follows:

Distance	Type of connection	Output High
15M	single wires	12V
15M-50M	twisted wires	15V
50M	twisted wires	24V

5.15 COMPONENTS

R1 - R34	34 x	121 Ω	1/8W
R35 - R68	34 x	46,4 KΩ	1/8W
R69 - R102	34 x	10 KΩ	1/8W
R103 - R136	34 x	4,64 KΩ	1/8W
R137 - R168	32 x	10 KΩ	1/8W
R169 - R170	2 x	681 Ω	1/8W
R171 - R172	2 x	261 Ω	1/8W
R173 - R174	2 x	21,5 KΩ	1/8W
R175 - R176	2 x	17,8 KΩ	1/8W
R177	1 x	215 KΩ	1/8W
R178	1 x	1 KΩ	1/8W
R179		12,1 Ω	1/8W
TS1 - TS67	66 x	BSX 20	
TS67 - TS68	2 x	BUY 47	
C1 - C34	34 x	330 pF	Ceramic plate
C35 - C68	34 x	1,5 nF	Ceramic plate
C69 - C100	32 x	100 pF	Ceramic plate
C101 - C102	2 x	100 pF	Ceramic plate
C103 - C120	18 x	3,9 nF	Ceramic plate
C121 - C122	2 x	0,47 µF	Moulded
C123	1 x	0,47 µF	Moulded
C124	1 x	0,47 µF	Moulded
Gr1 - Gr34	34 x	BAX 12	
Gr35-Gr68	34 x	BAX 13	
Gr69-Gr102	34 x 68 x	BZY 88 C6V2 for INIS HT Card BAX 12 for INiS LT Card	
U1-U3 (2nd channel)			
U10-U12	8 x	U6 A 7404 59 X	
U6-U9 (2nd channel)			
U15-U18	8 x	U6 B 7475 59 X	
U5	1 x	U6 A 7408 59 X	
U4	1 X	U7 B 9602 59 X	
SK1 - SK2	2 x	Switch	

Printed Circuit

Connector 00 6041 062 000 003

Connector 00 6041 050 000 003

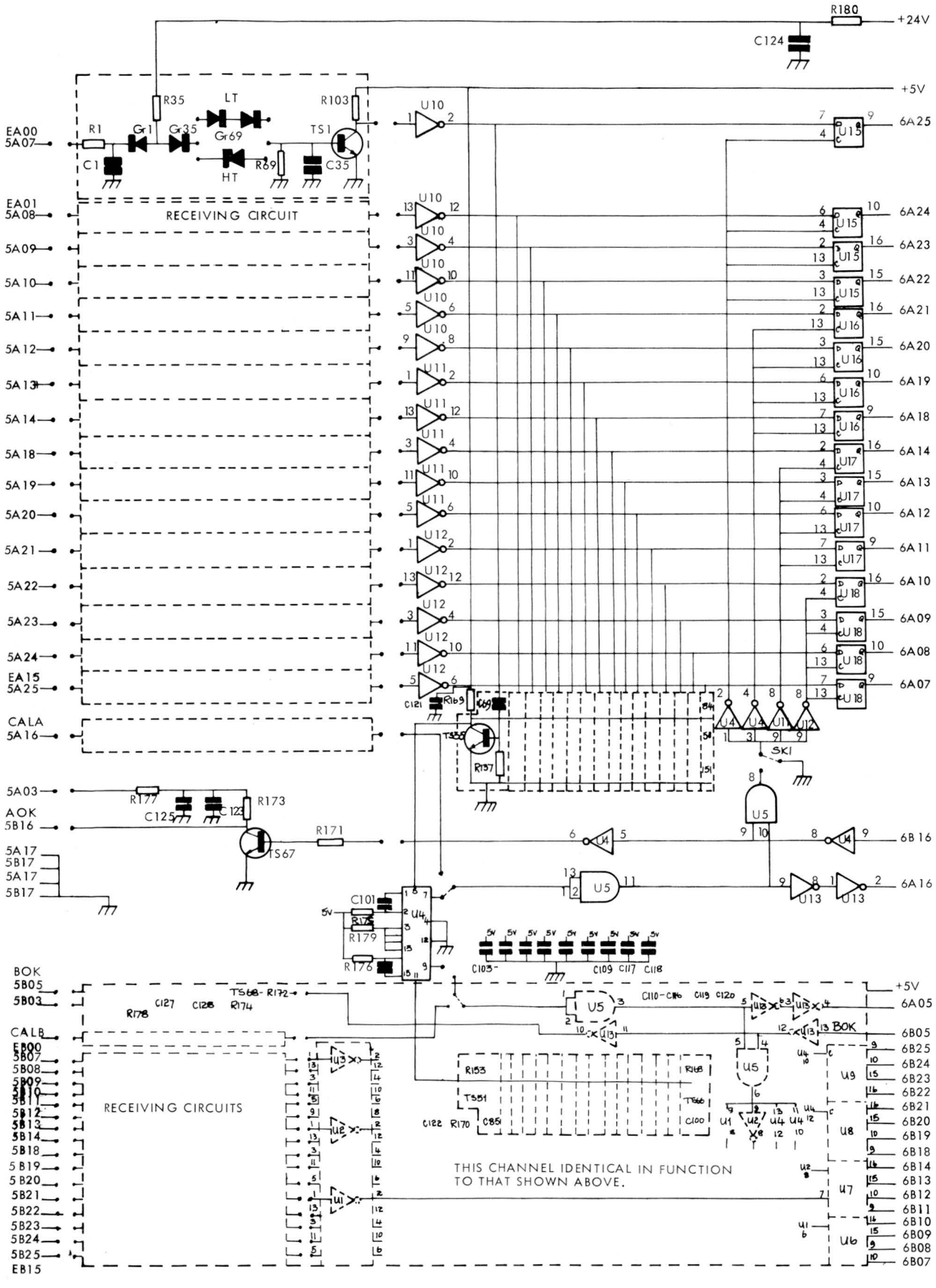


Figure 5.5 INIS CIRCUIT DIAGRAM

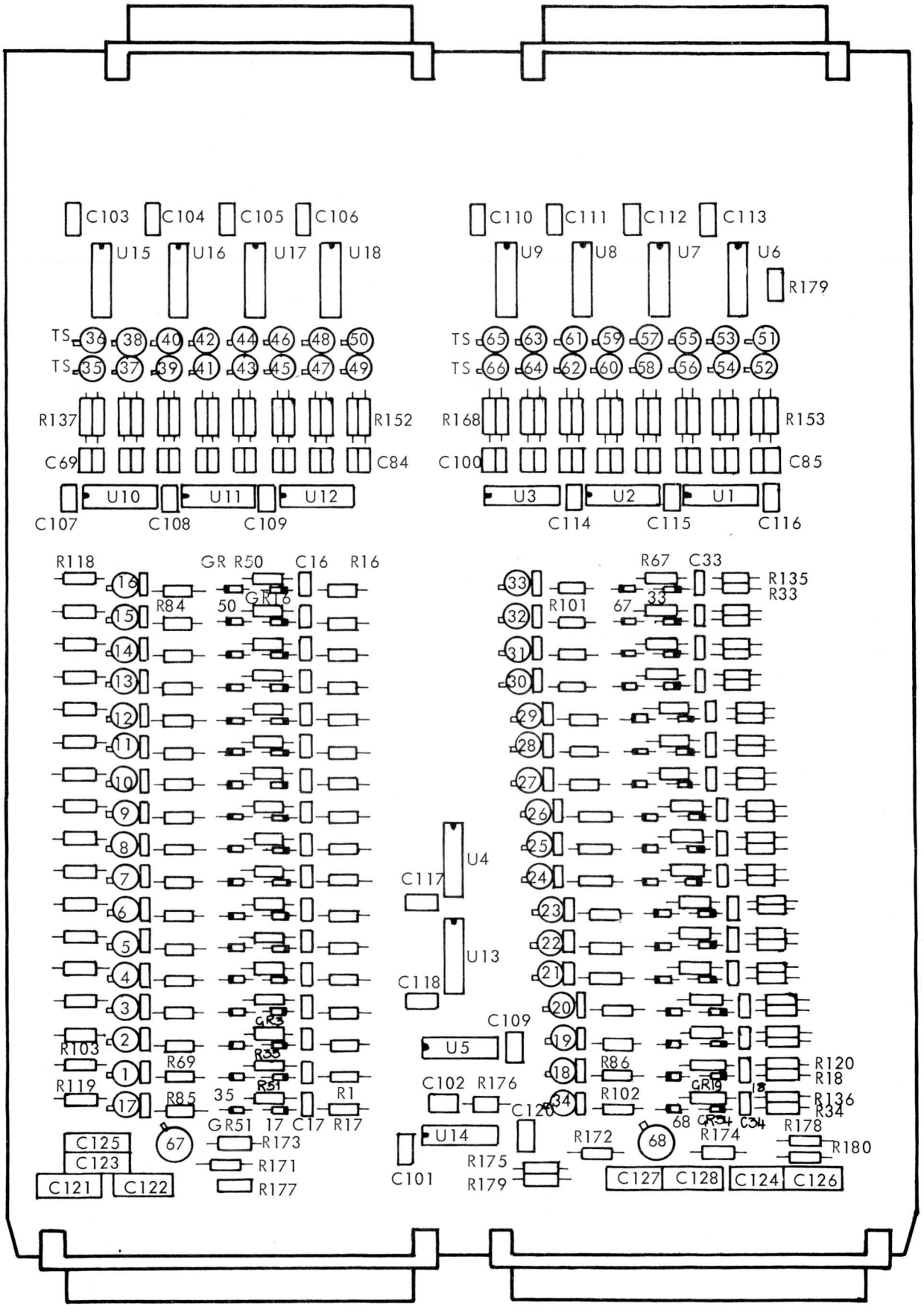


Figure 5.6 INIS CARD LAYOUT

5.16 SPECIAL CIRCUIT CARD-ONIS

The ONIS card may be used with either a DOC or the output channels of a DIOC to provide level adaptors to match the logic levels of the device to those of the DIOS. Each ONIS card provides the matching circuits for two output data channels and their control signals, and may be supplied in either of the following two forms.

(i) The ONIS Low Threshold (LT): to match the DIOS to devices with symetrical logic levels (e.g. high +6V, low -6V).

(ii) The ONIS High Threshold (HT): to match the DIOS to devices with asymetric logic levels (e.g. high +15V, low 0V).

5.17 Transmitting Circuits

The transmitting circuits provide the level adaptation for the data channels and response signals. The power for the transmitting circuits is supplied by the user and can be adjusted to give output voltages within the range:

high = 2.4V to 48V at 0.1mA

low = less than 0.4V max I = 50mA

The length of the cable connecting the ONIS card to the device sets a minimum value on these output voltages as follows:

Distance	Type of connection	Output High
15M	single wires	12V
15M-50M	twisted wires	15V
50M	twisted wires	24V

5.18 Receiving Circuits

The control signals CALA and CALB from the device are matched to the logic levels of the DIOS by the receiving circuits. With the low threshold option input signals can be in the range: High = +2.0V to +48V

Low = -48V to +0.4V

With the high threshold option input signals can be in the range:

High = +7.5V to 48V

Low = -48V to +4.5V

In both cases Isink at low level 1.8mA

Iload at high level 1.0uA

The length of the cable connecting the ONIS card to the device sets a minimum value on these input voltages as follows:

Distance	Connection	Noise Margin	ONIS	High	Low
15M	single wires	3V	LT	+5V	-2.2V
			HT	+10.5V	+1.5V
15 to 50	twisted wires	4V	LT	+6V	-3.2V
			HT	+11.5V	+0.5V
50M	twisted wires	6V			

5.19 COMPONENTS

C9 - C10	2 x	330pF ± 10% 100V	Ceramic plate
C11 - C12	2 x	1500pF ± 10% 100V	Ceramic plate
C1 - C8	8 x	0,1 µF ± 10% 100V	MPR
GR1 - GR2	6 x	BA X 12	
GR7 - GR8	2 x	BA X 13	
GR9 - GR10	2 x	BZ Y 88C6V2 (ONIS HT only)	
R1 - R34	34 x	261 Ω ± 1%	0,125W
R35 - R68	34 x	21,5 KΩ ± 1%	0,125W
R69 - R70	2 x	121 Ω ± 1%	0,125W
R71 - R72	2 x	46,4 KΩ ± 1%	0,125W
R73 - R74	2 x	4,64 KΩ ± 1%	0,125W
R75 - R76	2 x	10 KΩ ± 1%	0,125W
R77 - R78	2 x	12,1 Ω ± 1%	0,125W
TS1 - TS34	34 x	BUY 47	
TS35 - TS36	2 x	BS X20	
4	34 x	Transistor spacer 56245	
5	2 x	Transistor spacer 56246	
R79	1 x	Resistor 215 Ω ± 1%	0,125W

Printed circuit

Connector 00 6041 062 000 003

Connector 00 6041 050 000 003

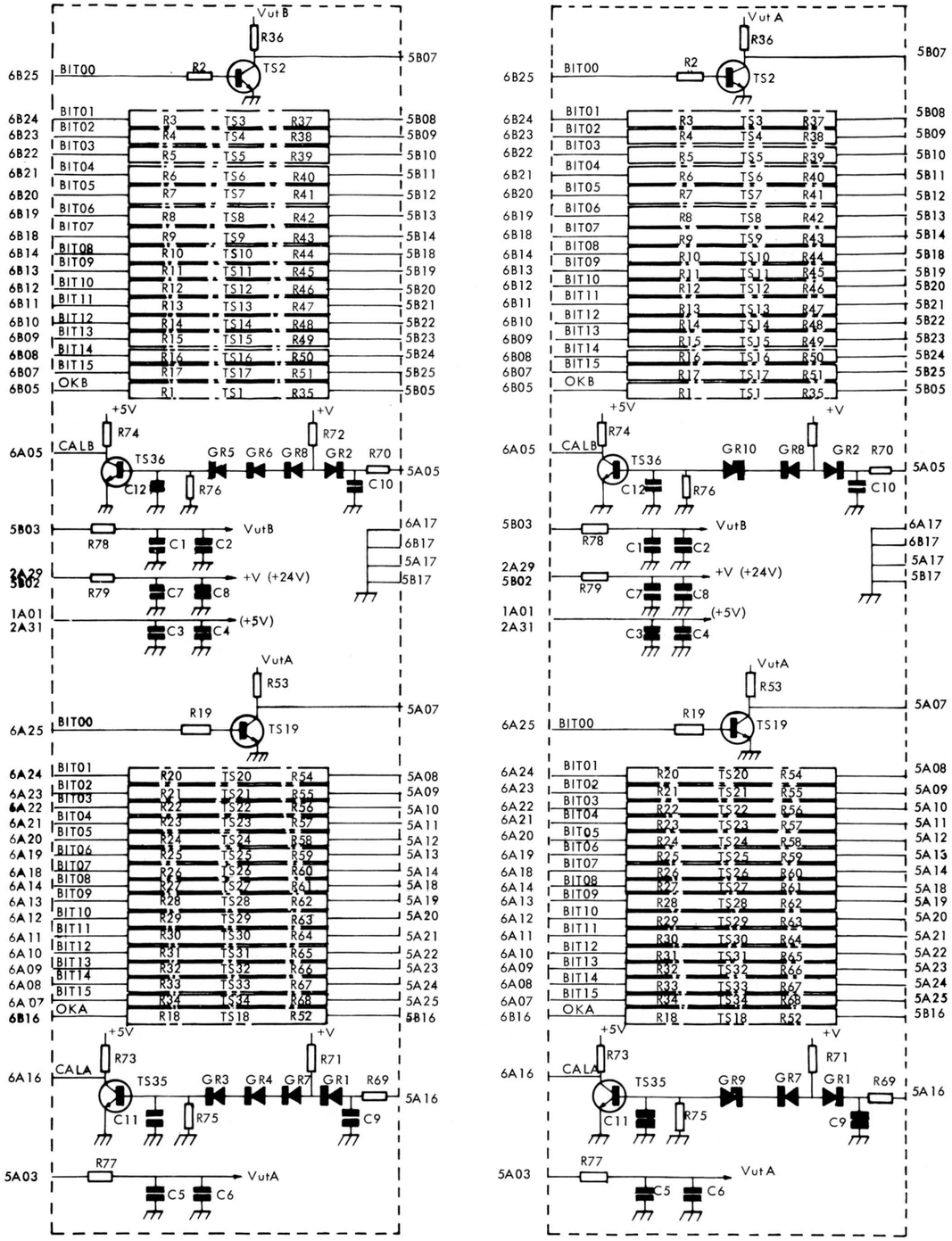


Figure 5.7 ONIS CIRCUIT DIAGRAM

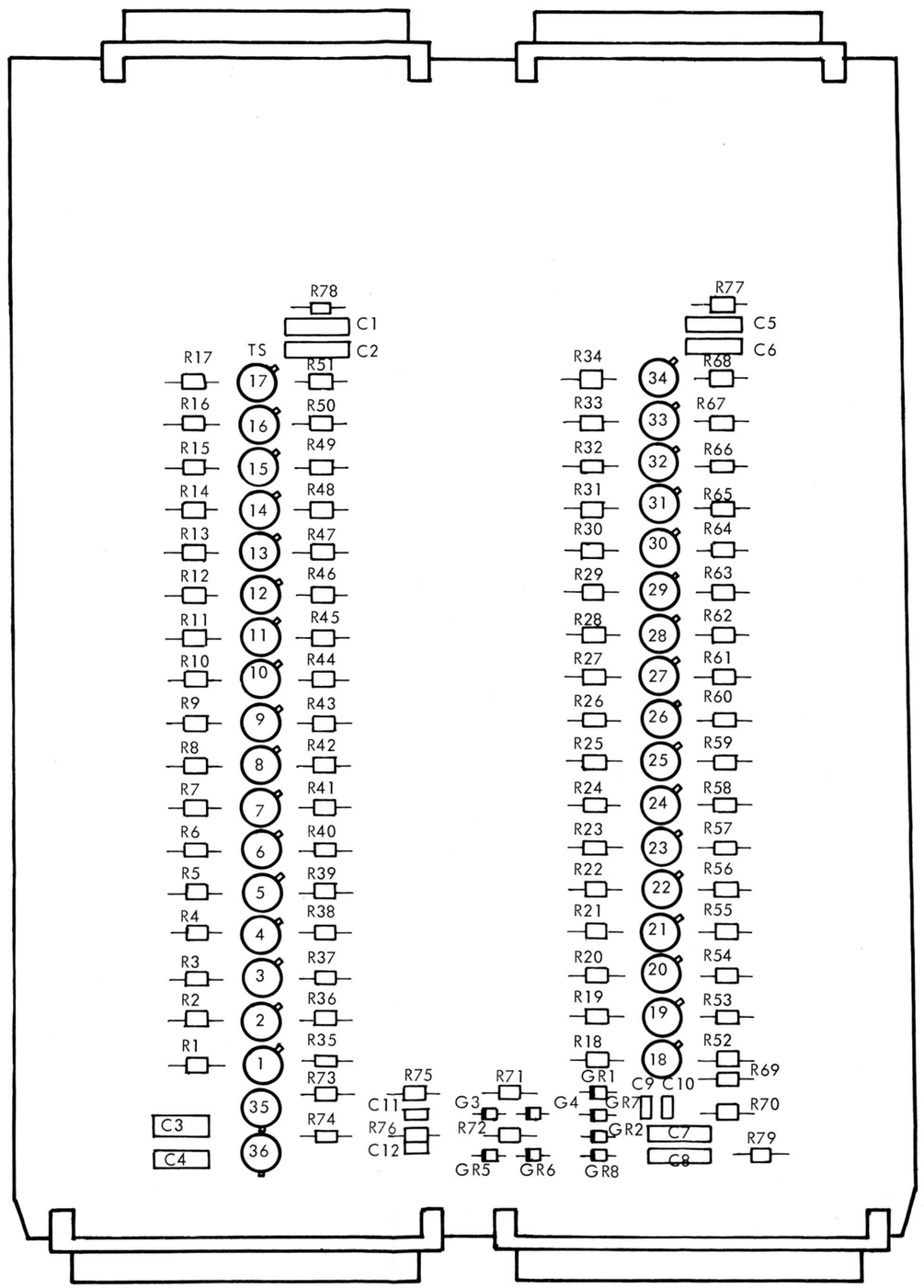


Figure 5.8 ONIS CARD LAYOUT

COMPONENTS LIST DIOC

Reference Number	Quantity	Description	12 NC - Code
D4 H7	2 x	IC U6A7400 59X	9331 765 30112
D3	1 x	IC U6A 7402 59X	9331 765 40112
D1 E1 F1 G1 H1	5 x	IC U6A 7403 59X	9331 765 50112
A1 A2 A3 B3 C1 C2 C3 C5 C6 C7 D7 E2 E7 D5 F2 F7 G2 H2 G5	19 x	IC U6A 7404 59X	9331 765 60112
D6	1 x	IC U6A 7408 59X	9331 765 70112
C4 D2 H6	3 x	IC U6A 7420 59X	9331 765 90112
B2	1 x	IC U6A 7430 59X	9331 766 00112
E3 E4 F3 F4 G3 G4 H3 H4	8 x	IC U6A 7450 59X	9331 766 20112
E5 F5	2 x	IC U6A 7460 59X	9331 766 40112
E6 F6 G6	3 x	IC U6A 7474 59X	9331 766 50112
A4 A5 A6 A7 B5 B6 B7 B4	8 x	IC U6A 7475 59X	9331 766 60112
H5 G7	2 x	IC U7B 9602 59X	9331 913 60112
C11-C12	2 x	10 µF 16V	2222 001 15109
C13-C26	14 x	0.1 µF 10% 100V	2222 344 90002
C27-C67	41 x	1500pF 10% 100V Ceramic plate	2222 630 01152
C2 C4 C6 C8 C9 C10	6 x	3300pF + 10% 100V Ceramic plate	2222 630 01332
C1 C3 C5 C7	4 x	330pF + 10% 100V Ceramic plate	2222 630 01331
R1-R8	8 x	464 ohm + 1% 0.125W	5122 000 00961
R9 R10 R11 R12	4 x	1 Kohm + 1% 0.125W	5122 000 01041
R13-R16	4 x	17.8 K + 1% 0.125W	5122 000 01341
X1-X28	28 x	Test pin PFT 241	2411 025 07051
CV1 - CV12	12 x	Link CV 213	2411 024 01007
Printed circuit	1 x		5111 100 03673
Connector 006041 062 000 002	2 x		2422 022 98012
Connector 006041 050 000 002	2 x		2422 022 98014

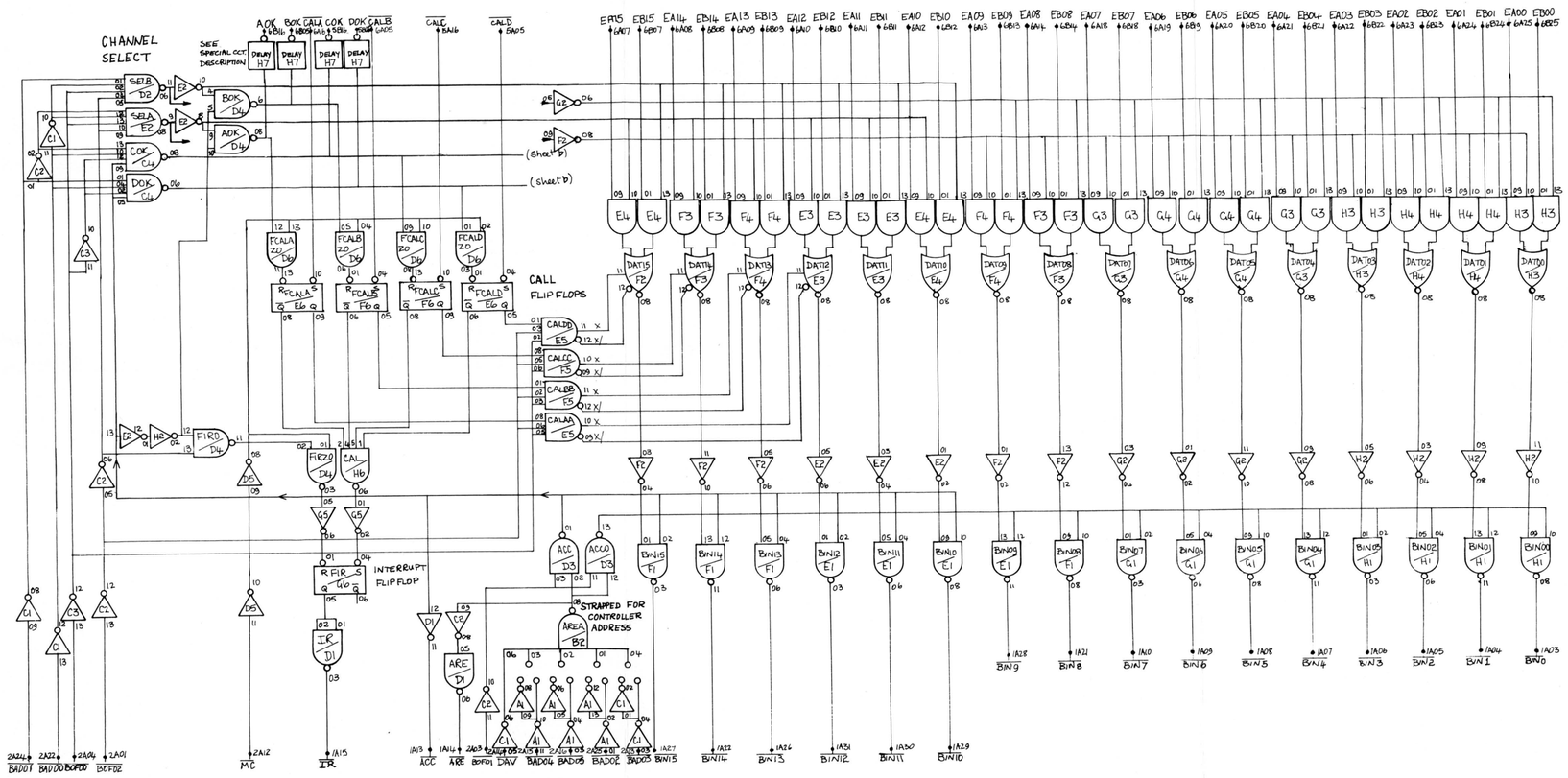


Figure 5.10 DIOC: INPUT CHANNELS AND CONTROL LOGIC

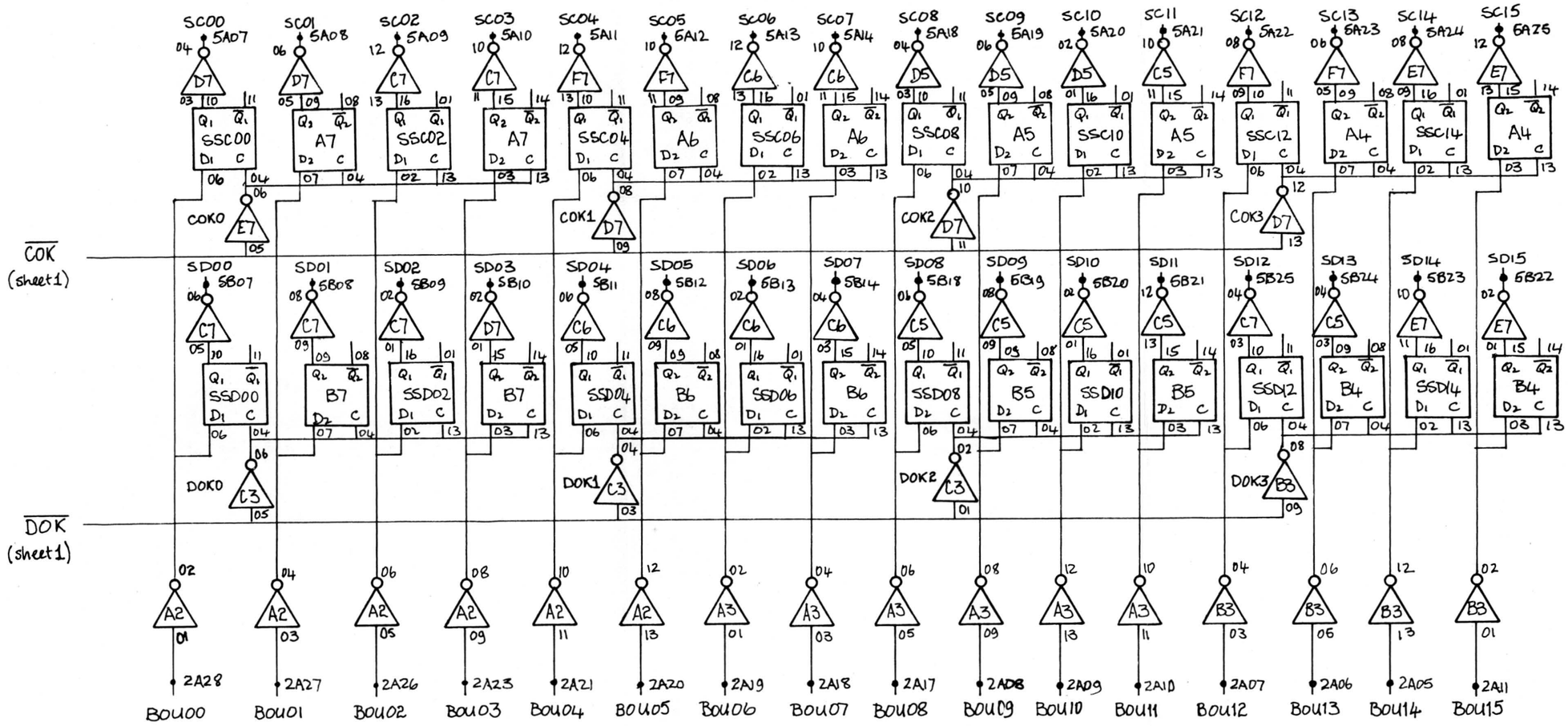


Figure 5.11 DIOC: OUTPUT CHANNELS

COMPONENTS LIST DIC

Reference Number	Quantity	Description	12 NC - Code
G3	1 x	IC 7400	5111 000 00011
D1 E1 F1 G1 H1	5 x	IC 7403	5111 000 00041
A1 C1 E2 F2 G2 H2 D3 E3 C4 D4 G4	11 x	IC 7404	5111 000 00051
C3	1 x	IC 7408	5111 000 00071
C2 E4 F4	3 x	IC 7410	5111 000 00081
B2	1 x	IC 7420	5111 000 00121
A2	1 x	IC 7430	5111 000 00131
A5 A6 B5 B6 C5 C6 D6 E5 E6 F5 F6 G5 G6 H5 H6	16 x	IC 7453	5111 000 00181
A4 B4	2 x	IC 7460	5111 000 00191
A3 B3 D2	3 x	IC 7474	5111 000 00221
F3 H3	2 x	IC 9602	5111 000 00571
C1 C2	2 x	10 µF 16V	2222 001 15109
C3 - C14	12 x	0.1 µF ± 10% 100 V MPR	2222 344 90002
C15 - C58	44 x	1500 PF ± 10% 100 V Ceramic plate	2222 630 01152
C59 - C62	4 x	330 PF ± 10% 100 V Ceramic plate	2222 630 01331
C63 - C68	6 x	3300PF ± 10% 100 V Ceramic plate	2222 630 01332
R15 - R18	4 x	17.8 Ω ± 1% 0.125 W	5122 000 01341
R1 - R14	14 x	1 KΩ ± 1% 0.125W	5122 000 01041
R19 - R34	16 x	3K16 ± 1% 0.125W	5122 000 01161
R35 - R50	16 x	6K19 ± 1% 0.125W	5122 000 01231
CV1 - CV12	12 x	CV 213	2411 024 01007
X1 - X28	28 x	PTF 241	2411 025 07051
Printed Circuit	1 x		5111 100 04392
Connector 6041 062 000 003	2 x		2422 022 98012
Connector 6041 050 000 003	2 x		2422 022 98014

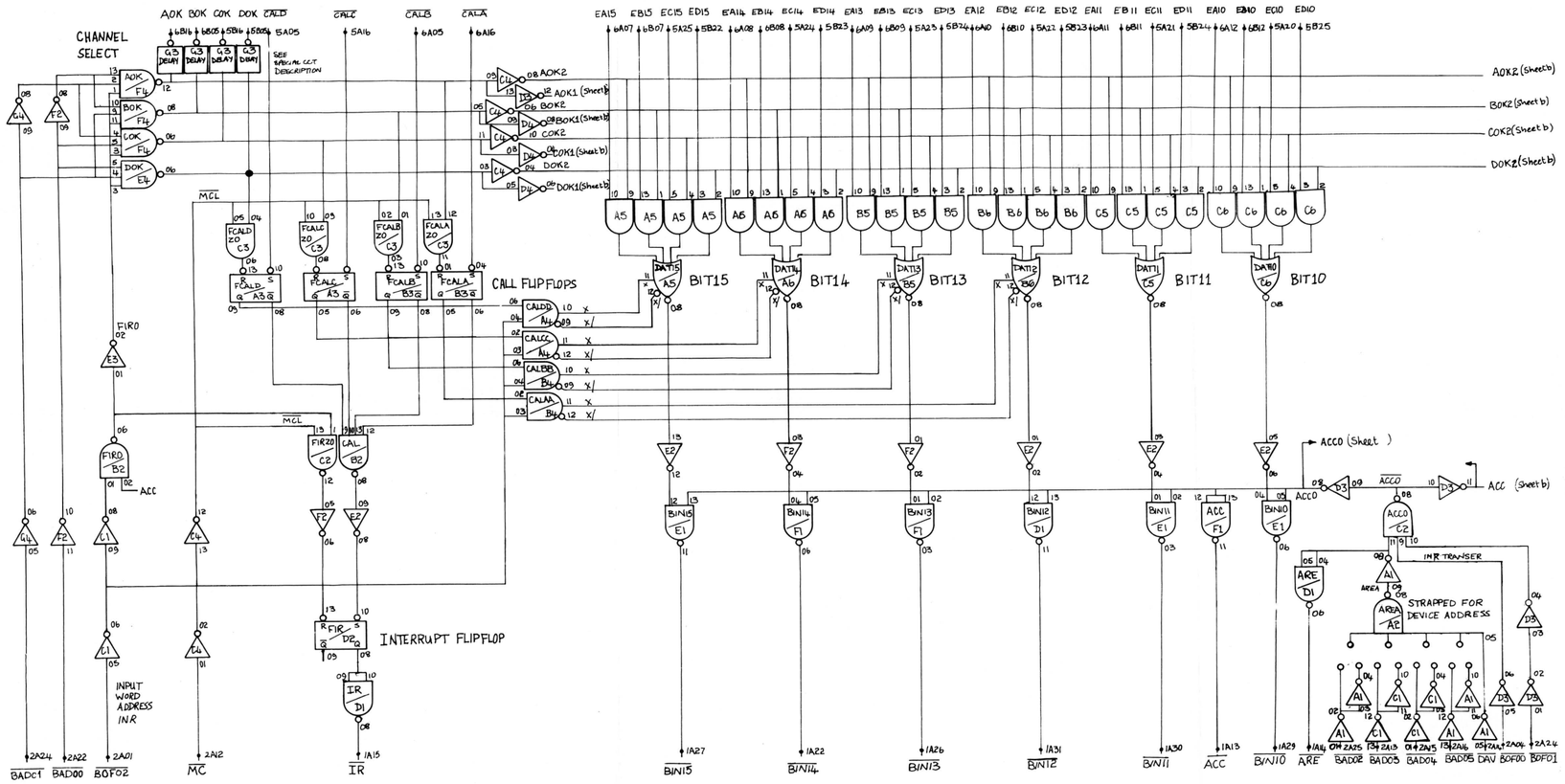


Figure 5.13 DIGITAL INPUT CONTROLLER (DIC)

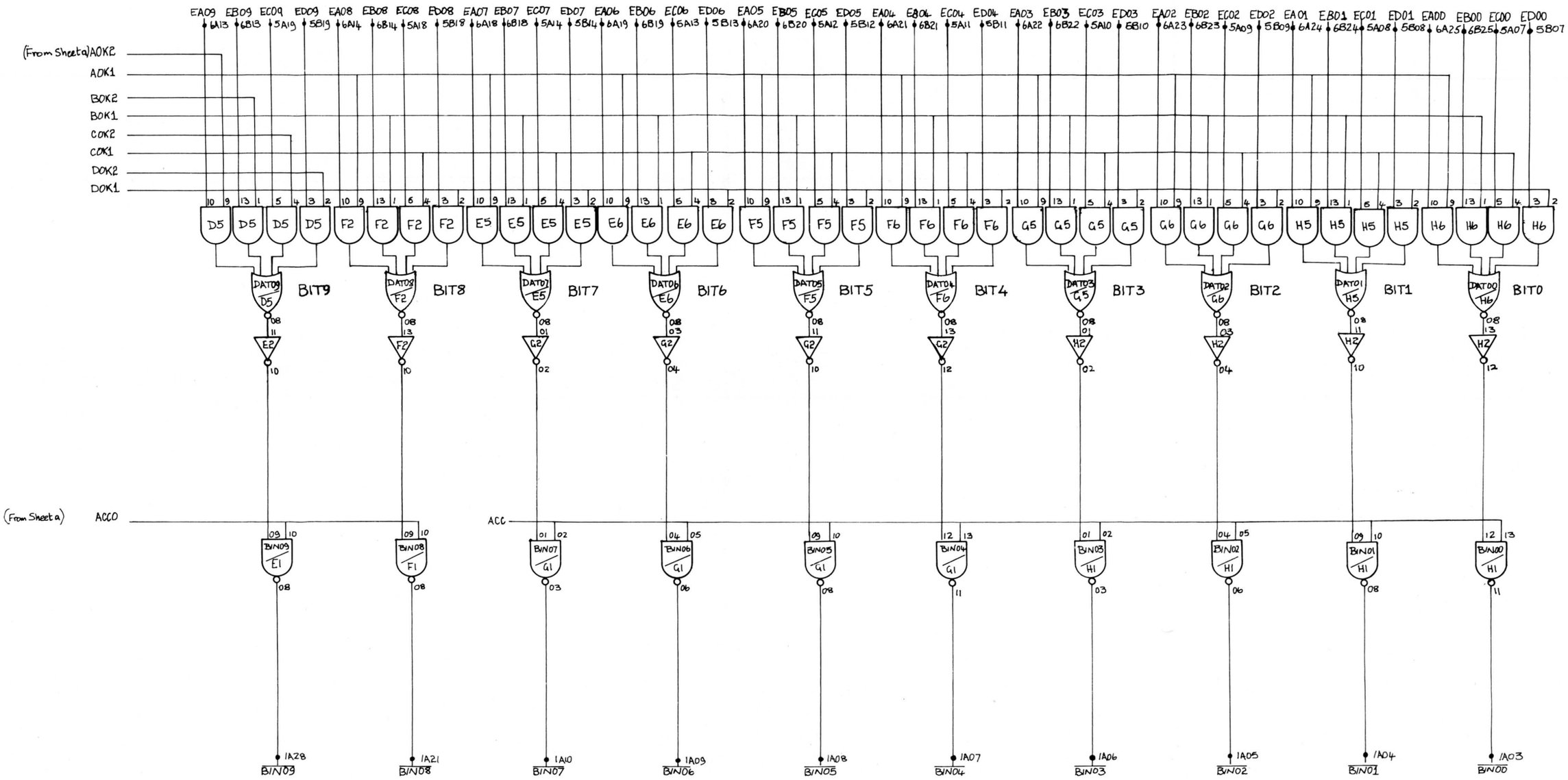


Figure 5.14 DIGITAL INPUT CONTROLLER

Reference Number	Quantity	Description	12 NC - Code
G2 F3	2 x	IC 7400	5111 000 00011
F1 G1	2 x	IC 7403	5111 000 00041
A1 A4 B1 B3 B4 B7 C2 C4 C7 D4 D7 E1 E4 E7 F2 F7 G4 G7 H4 H7	22 x	IC 7404	5111 000 00051
D2	1 x	IC 7408	5111 000 00071
D3	1 x	IC 7410	5111 000 00081
C3 E2 H3	3 x	IC 7420	5111 000 00121
A3	1 x	IC 7430	5111 000 00131
D1 H1 H2	3 x	IC 7474	5111 000 00221
A5 A6 B5 C5 C6 D5 D6 E5 E6 F5 F6 G5 G6 H5 H6	16 x	IC 7475	5111 000 00231
C1 - C14	14 x	0.1 µF 10% 100V MPR	2222 344 90002
C15 - C59	39 x	1500pF ± 10% 100V Ceramic plate	2222 630 01152
C54 - C59	6 x	3300pF ± 10% 100V Ceramic plate	2222 630 01332
C60 - C63	4 x	330pF ± 10% 100V Ceramic plate	2222 630 01331
R14 - R17	4 x	17.8Kn ± 1% 0.125W	5122 000 01341
R4 - R13	10 x	1Kn ± 1% 0.125W	5122 000 01041
R18	1 x	3.16Kn ± 1% 0.125W	5122 000 01161
R19	1 x	6.19Kn ± 1% 0.125W	5122 000 01231
X1 - X28	28 x	FPT 241	2411 025 07051
CV1 - CV12	12 x	CV 213	2411 024 01007
C64 - C65	2 x	10µ F 16V	2222 001 15109
G3 E3	2 x	IC 9602	5111 000 00571
Printed circuit	1 x		5111 100 04402
Connector 6041 062 000 003	2 x		2422 022 98012
Connector 6041 050 000 003	2x		24 22 022 98014

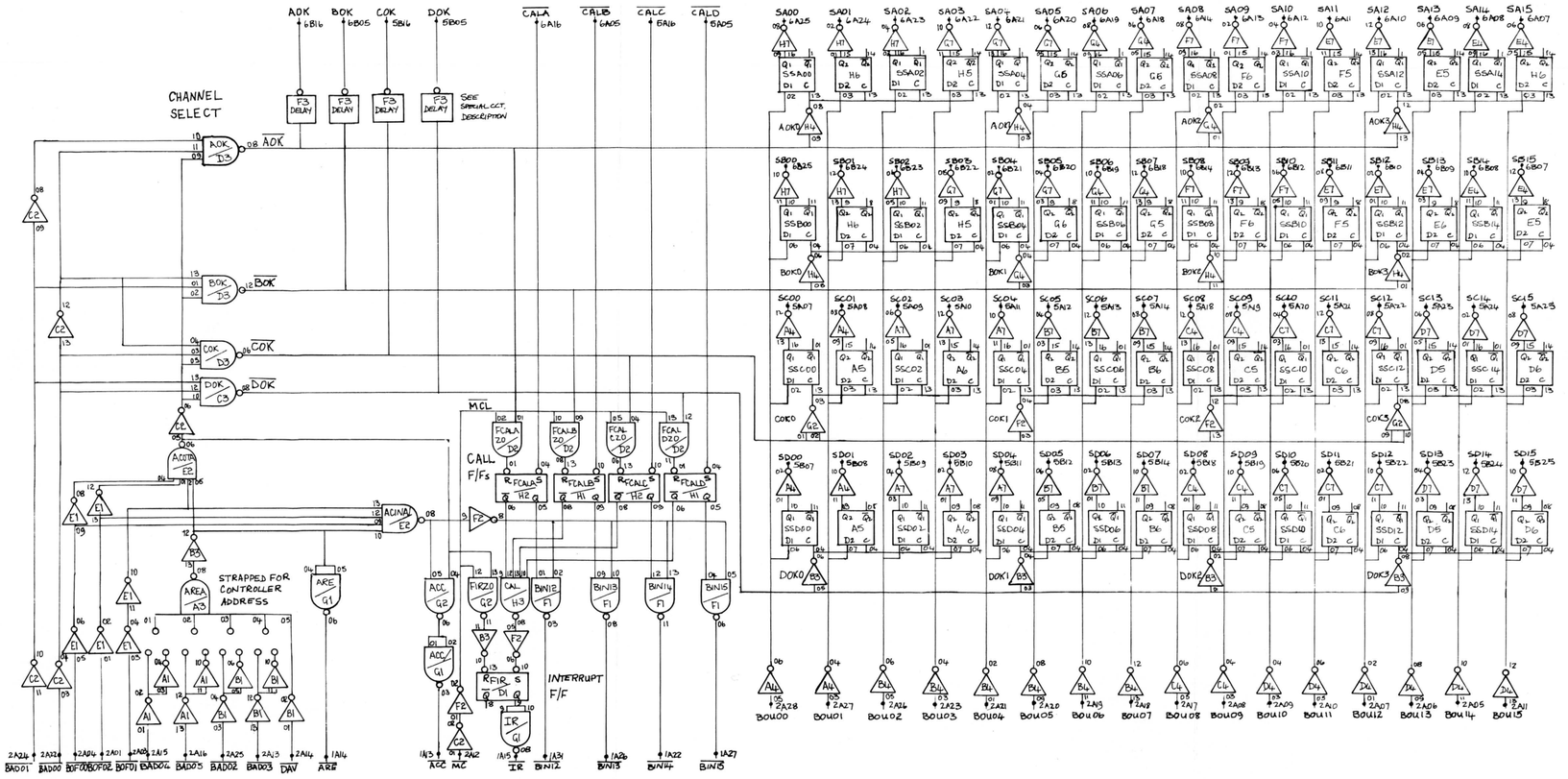


Figure 5.16 DIGITAL OUTPUT CONTROLLER(DOC)

SECTION VI

LINE PRINTER CONTROL UNIT

BRIEF DESCRIPTION

The Line Printer Control Unit provides the interface and control logic to transfer information from the central processor to the Line Printer. The control unit may be used with either the programmed channel or the multiplex channel of the central processor; the mode is selected prior to installation and is not program changeable. The control unit is contained on one card and may be used with either of the following line printers:

Data Products model 2310

Data Products model 2410 or 2420

Data Products model 2440

Figure 6.2 is a Block Diagram of the control unit.

6.1 PRINT COMMANDS

The format of the data sent is seven bit (Output Bus lines BOU15-09) plus one Paper Instruction (PI) indicator on BOU08. If the PI bit is zero the other seven bits are loaded into the Line Printer's buffer and eventually printed with the exception of the following three characters which are decoded by the line printer as commands:

MNEMONIC	MEANING	CODE
PF	Paper Feed - advances the paper one line and causes a CR	BOU 15 14 13 12 11 10 9 8 0 1 0 1 0 0 0 0
FF	Form Feed - advances the paper to the top of the next sheet of paper and gives a CR	0 0 1 1 0 0 0 0
CR	Carriage Return - sets the printer at the left-most print position	1 0 1 1 0 0 0 0

If the PI bit is one then the other seven bits are considered to be a vertical format character. This character indicates to the Line Printer that the paper must be moved either to a position indicated by the character itself or by the Line Printer's control paper tape. If bit 11 is zero the line printer advances

the paper until the next hole is encountered in the control paper tape channel specified by bits 15 - 13.

BOU	15	14	13	12	11	10	9	8
Paper tape channel No.	0	0	X	1	1			

If bit 11 is one the line printer advances the paper the number of lines specified by bits 15 -12.

BOU	15	14	13	12	11	10	9	8
Number of lines Skipped	1	X	1	1				

6.2 ADDRESSING

The address of the control unit may be selected using straps which connect the address decode gate in the CU to the computer BAD lines BAD00-05. The address part of instructions is checked when a validity signal DAV/ is received from the computer. If the address is accepted the signal ARE/ is returned to the computer and command decoding is enabled.

6.3 COMMAND DECODING

The setting of the bits on BOF lines 00-02 determine the function of instructions sent to the controller. These bits are decoded by the 1 out of 10 decoder module 9301 the signal AREA/ enables the decoding once the CU's address has been recognised. The commands recognised by the control unit are:

BOF 00	01	02	COMMAND	OPERATIONAL STATE REQUIRED	FUNCTION
1	1	0	Test Status	Any	To determine the status of the control unit
0	1	1	CIO Start	Inactive	To initiate the transfer of a block of information
0	1	0	CIO Stop	Any	Halt CPU/CU transfer
0	0	X	OTR Command	Exchange	To transfer one 8-bit character
1	1	1	SST Send Status	Wait Status	Transfer line printers status to CPU

X the setting of this bit is not important.

The signal ACC/ is returned to the CPU when the command is recognised.

6.4 OPERATIONAL STATES

The control unit functions in four operational states (INACTIVE, EXCHANGE, EXECUTE and WAIT STATUS) and switches between them as a result of signals received from either the CPU or the device. Figure 6.3 shows the interworking of the operational states. The code shown on thediagram next to the name of each state is the true output from the Operational State Register (flip flops F0 and F1) which determine the state of the controller.

INACTIVE This is an idle condition for the CU to which it returns after completing the transfer of a block of information to the printer (see WAIT STATUS). The command CIO START is required, if the CU is in the INACTIVE state, to initiate a data transfer. Provided the line printer is OPERABLE the command toggles both the F0 and F1 flip flops putting the control unit into EXCHANGE state, otherwise the Halt flip flop is set and the control unit is switched into the WAIT STATUS state. The CIO START command can only be received while the CU is in the INACTIVE state.

EXCHANGE The EXCHANGE state is used to load one eight bit character from the CPU output bus into the Output Buffer in the CU and to prepare the CU to transfer this character to the line printer. As soon as the CU switches to the EXCHANGE state an interrupt (PIL/) or Break Request (BR/) if the CU is connected to the multiplex channel, is sent to the processor to request a data transfer. The CPU responds to the request with an OTR Output command and places the data for transfer on BOU lines 08-15. The OTR command (ACOTR/) clocks the data on the BOU lines into the CUs Output Buffer, sets the Strobe flip flop and puts the CU into the EXECUTE state.

EXECUTE This state is used to transfer the data from the CU to the Line Printer and to receive requests from the printer for further data transfers. When the CU switches to the EXECUTE state the signal EXT/goes low and with FSTROBE/ produces the STROBE signal to transfer the data from the Output Buffer to the Line Printer. The Line Printer stores each printable character transferred and sends demands for new characters until either its buffer is full or until a print command is received from the control unit. In both cases the line printer prints the contents of its buffer and in the latter case also obeys the print command afterwards. The DEMAND signal received

from the printer resets the FSTROBE flip flop and sets the Operational State Register back into EXCHANGE state; this causes a new character request to be sent to the CPU.

WAIT STATUS The CU uses WAIT STATUS to transfer a status word to the CPU. It is normally entered from the EXCHANGE state after the CPU has either sent the last character with an End of Range (EOR) signal, for multiplex channel transfers, or a CIO STOP command, for program channel transfers. WAIT STATUS is also entered if the Line Printer becomes inoperable. All of these conditions cause the HALT flipflop to be set which sends a Status Request Interrupt (PIL/) to the CPU. The control unit must then wait for a Send Status (SST/) command from the processor to place the device status on the Input Bus line BIN15. BIN15 is set if the Line Printer is not operable: BIN lines 14-08 have no significance. The command SST sets the control unit into the INACTIVE state and resets both the HALT and STROBE flip flops.

6.5 RESETTING

A Master Clear signal (MC/) may be sent from the processor to reset both the Halt and Strobe flip flops and to set the Operational State register into the INACTIVE state.

6.6 INTERRUPTS

If the control unit is connected to the multiplex channel a DEMAND signal received from the Line Printer will cause a Break Request signal (BS/). If the program channel is used the signal is strapped across to give a program interrupt (PIL/) (see EXECUTE). Regardless of whether the program channel of multiplex channel is used a program interrupt (PIL/) is used as a status request whenever the Halt flip flop is set (see WAIT STATUS). Setting the Halt flip flop prevents demands from the line printer from causing are interrupt or break request.

6.7 TEST STATUS

The Test Status command may be sent to determine if the control unit is busy. It is always accepted and BIN15 is set to a one if the CU is not in the INACTIVE state.

6.8 CU TO LINE PRINTER CONNECTIONS

Connections between the control unit and the line printer are made using twisted pair wires between ELCO connectors. One of the wires is connected to ground both at the CU and at the line printer and the other is connected to the appropriate signal.

6.9 TIMING

Figure 6.4 shows the sequence of operations required to initiate and continue a data transfer from the CPU to the Line Printer. Figure 6.5 shows the status request and sending sequence.

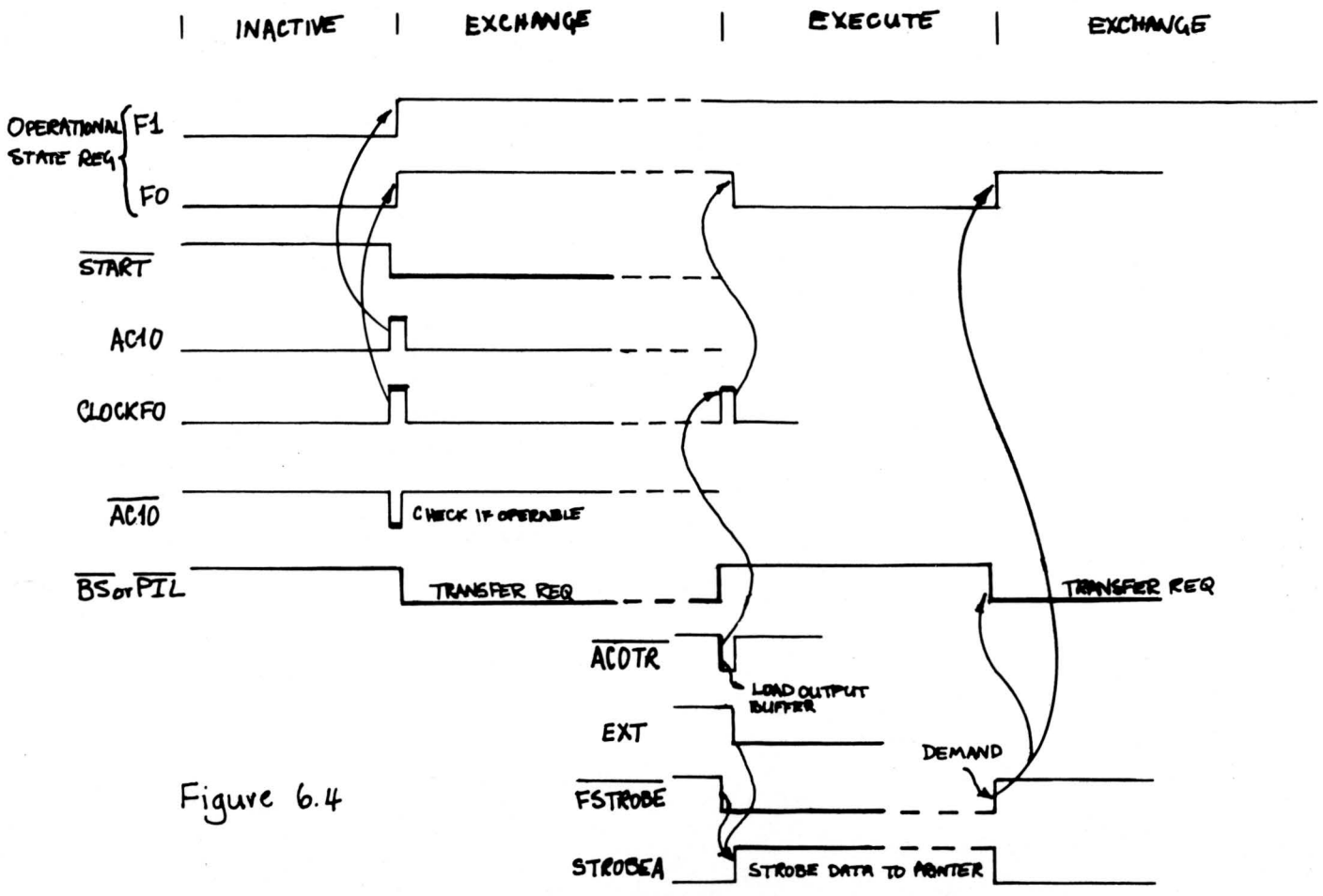


Figure 6.4

The EXCHANGE/EXECUTE cycle is repeated until all the data has been transferred. If the data transfer is controlled by the program channel a HALT command will normally be programmed at the end of the transfer. An EOR (End of Range) signal is used in place of the HALT instruction when the multiplex channel is used for the transfer.

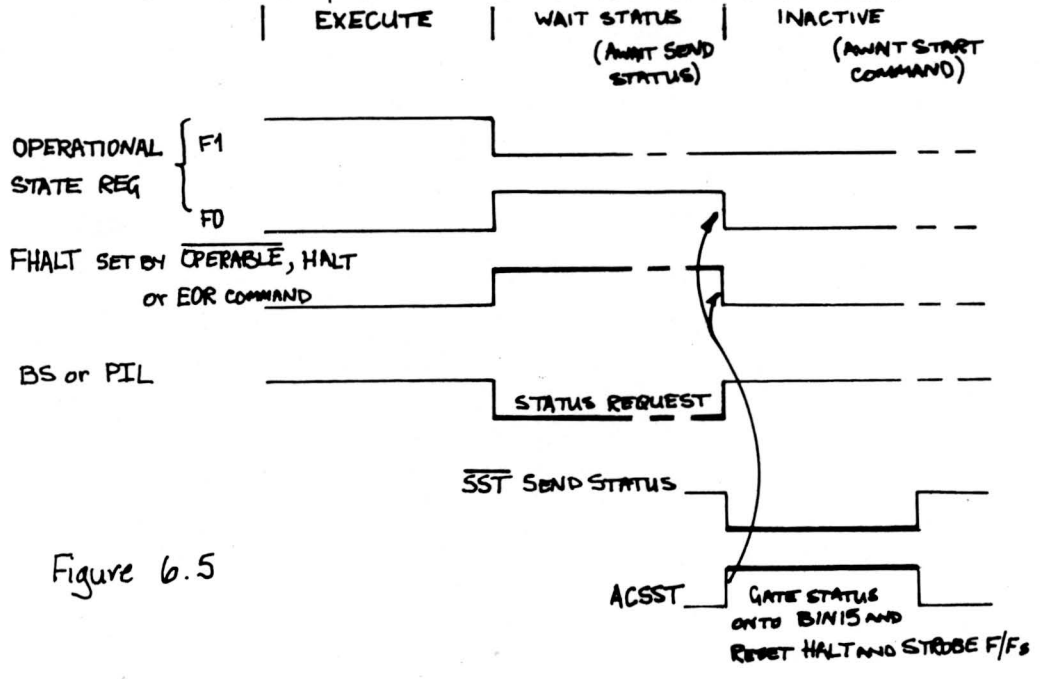


Figure 6.5

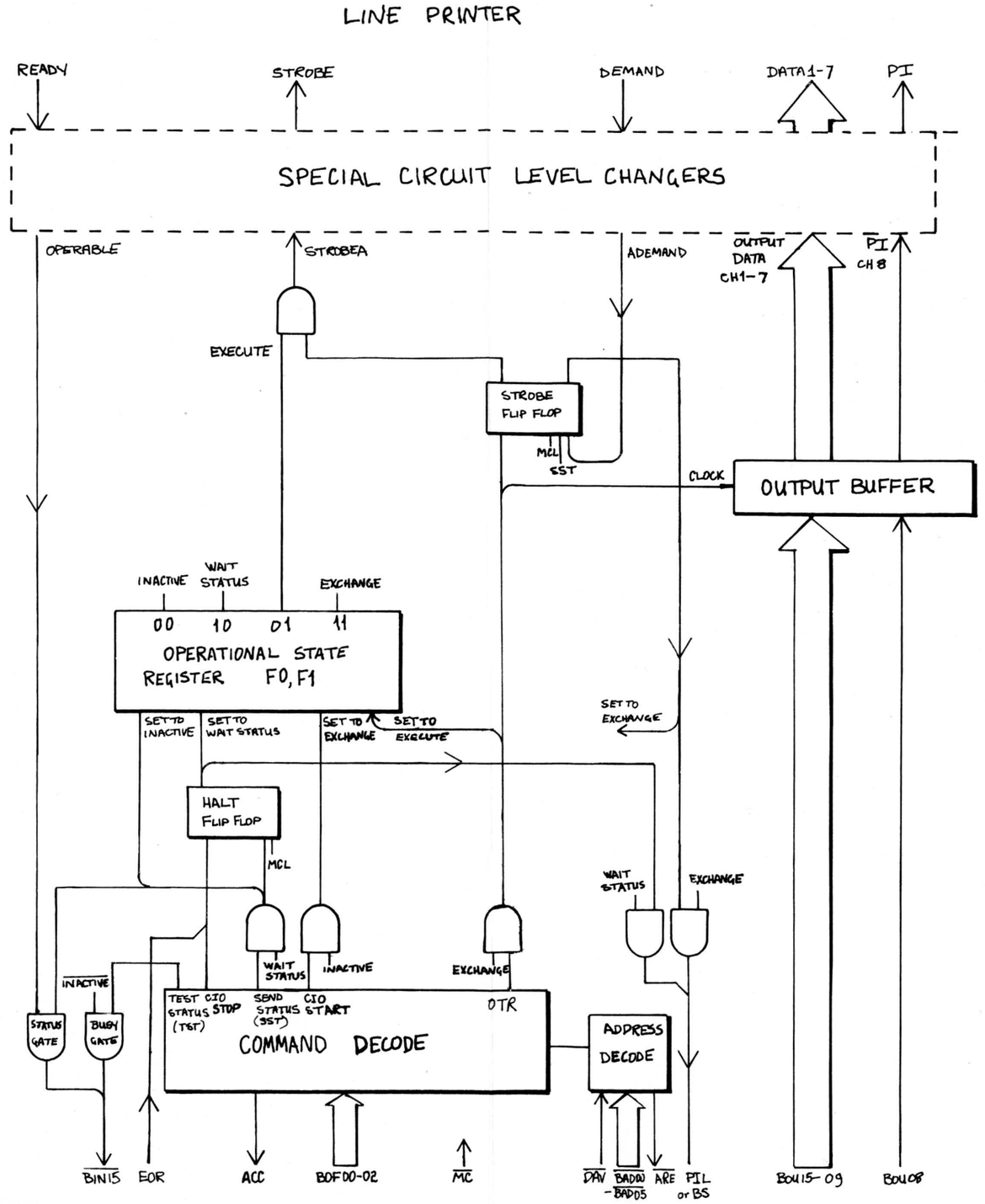
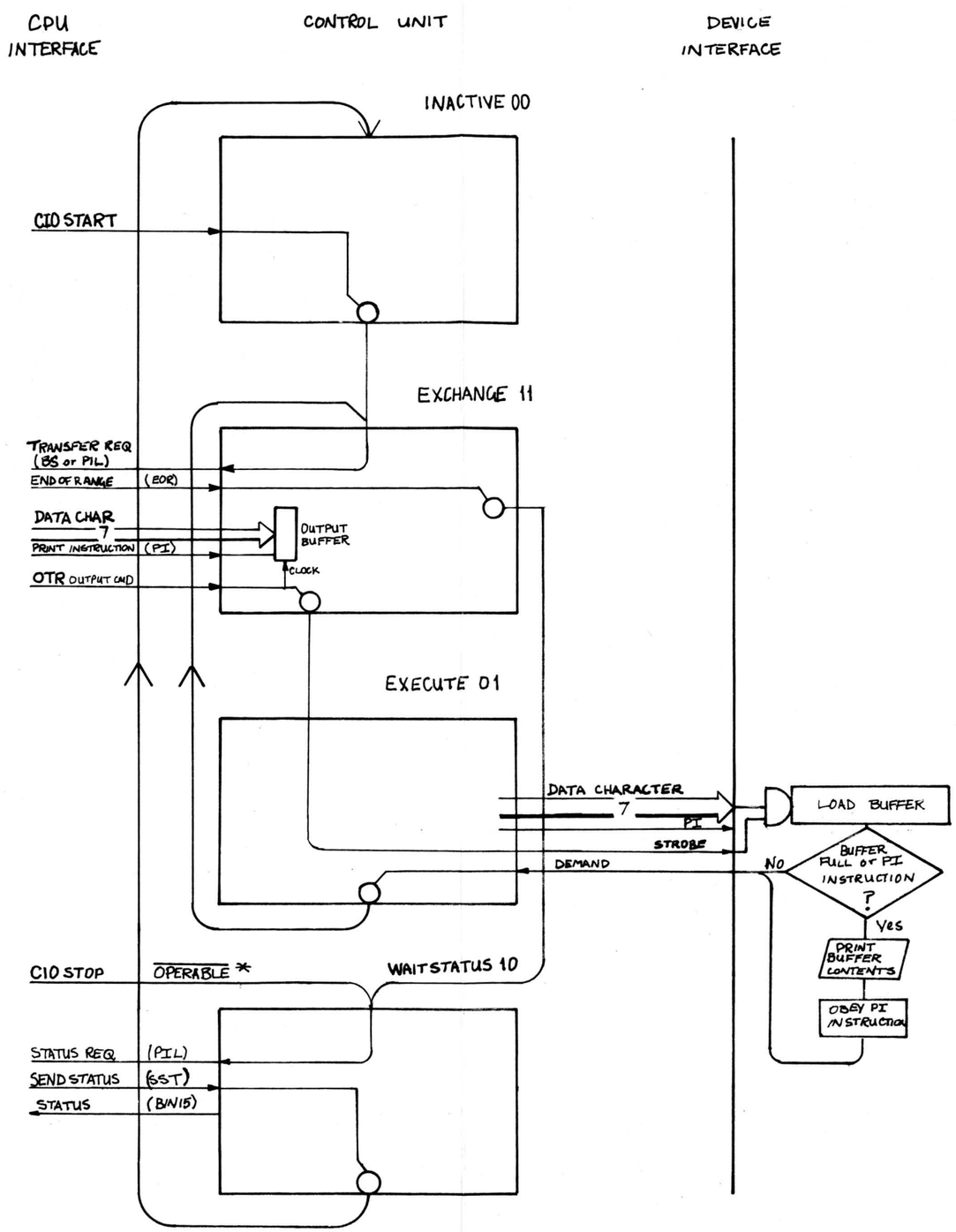


Figure 6.2 BLOCK DIAGRAM



* THESE SIGNALS MAY BE RECEIVED WHILE THE CONTROLLER IS IN ANY OF THE OTHER THREE OPERATIONAL STATES.

Figure 6.3 OPERATIONAL STATES

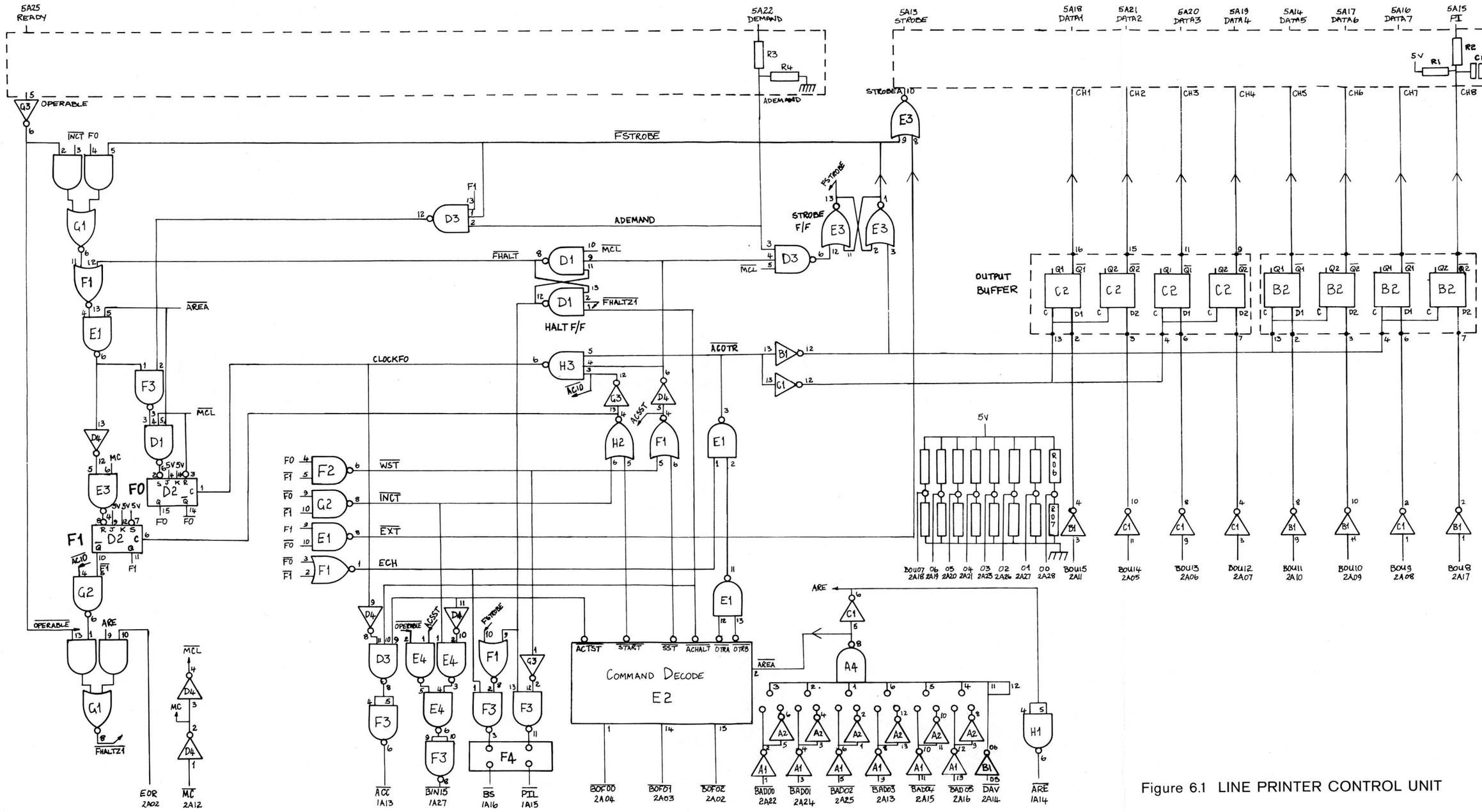


Figure 6.1 LINE PRINTER CONTROL UNIT